

**K9L8G08U1A  
K9G4G08U0A K9G4G08B0A**

**Preliminary  
FLASH MEMORY**

# K9XXG08XXA

勝特力材料 886-3-5753170  
勝特力电子(上海) 86-21-34970699  
勝特力电子(深圳) 86-755-83298787  
[Http://www.100y.com.tw](http://www.100y.com.tw)

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**FLASH MEMORY**

## Document Title

**512M x 8 Bit / 1G x 8 Bit NAND Flash Memory**

## Revision History

| <u>Revision No</u> | <u>History</u>  | <u>Draft Date</u> | <u>Remark</u> |
|--------------------|---|-------------------|---------------|
| 0.0                | 1. Initial issue  | May. 2nd 2006     | Advance       |
| 0.1                | 1. Add 2.7V part<br>2. Add note of command set table<br>3. Add nWP timing guide<br>4. Endurance 10K -> 5K | Sep. 25st 2006    | Preliminary   |

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**Preliminary**  
**FLASH MEMORY**
**512M x 8 Bit / 1G x 8 Bit NAND Flash Memory**
**PRODUCT LIST**

| Part Number  | Vcc Range   | Organization | PKG Type |
|--------------|-------------|--------------|----------|
| K9G4G08B0A   | 2.5V ~ 2.9V | X8           | MCP(TBD) |
| K9G4G08U0A-P | 2.7V ~ 3.6V |              | TSOP1    |
| K9G4G08U0A-I |             |              | 52ULGA   |
| K9L8G08U1A-I |             |              |          |

**FEATURES**

- Voltage Supply
  - 2.7V Device(K9G4G08B0A) : 2.5V ~ 2.9V
  - 3.3V Device(K9G4G08U0A) : 2.7V ~ 3.6V
- Organization
  - Memory Cell Array : (512M + 16M) x 8bit
  - Data Register : (2K + 64) x 8bit
- Automatic Program and Erase
  - Page Program : (2K + 64)Byte
  - Block Erase : (256K + 8K)Byte
- Page Read Operation
  - Page Size : (2K + 64)Byte
  - Random Read : 60μs(Max.)
  - Serial Access : 30ns(Min.)
- Memory Cell : 2bit / Memory Cell
- Fast Write Cycle Time
  - Program time : 800μs(Typ.)
  - Block Erase Time : 1.5ms(Typ.)
- Command/Address/Data Multiplexed I/O Port
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
  - Endurance : 5K Program/Erase Cycles(with 4bit/512byte ECC)
  - Data Retention : 10 Years
- Command Register Operation
- Unique ID for Copyright Protection
- Package :
  - K9G4G08U0A-PCB0/PIB0 : Pb-FREE PACKAGE
  - 48 - Pin TSOP1(12 x 20 / 0.5 mm pitch)
  - K9G4G08U0A-ICB0/IIB0
  - 52 - Pin ULGA (12 x 17 / 1.00 mm pitch)
  - K9L8G08U1A-ICB0/IIB0
  - 52 - Pin ULGA (12 x 17 / 1.00 mm pitch)
  - K9G4G08B0A : MCP(TBD)

**GENERAL DESCRIPTION**

Offered in 512Mx8bit, the K9G4G08X0A is a 4G-bit NAND Flash Memory with spare 128M-bit. The device is offered in 2.7V and 3.3V Vcc. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. A program operation can be performed in typical 800μs on the 2,112-byte page and an erase operation can be performed in typical 1.5ms on a (256K+8K)byte block. Data in the data register can be read out at 30ns cycle time per byte. The I/O pins serve as the ports for address and data input/output as well as command input. The on-chip write controller automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. Even the write-intensive systems can take advantage of the K9G4G08X0A's extended reliability of 5K program/erase cycles by providing ECC(Error Correcting Code) with real time mapping-out algorithm. The K9G4G08X0A is an optimum solution for large nonvolatile storage applications such as solid state file storage and other portable applications requiring non-volatility.

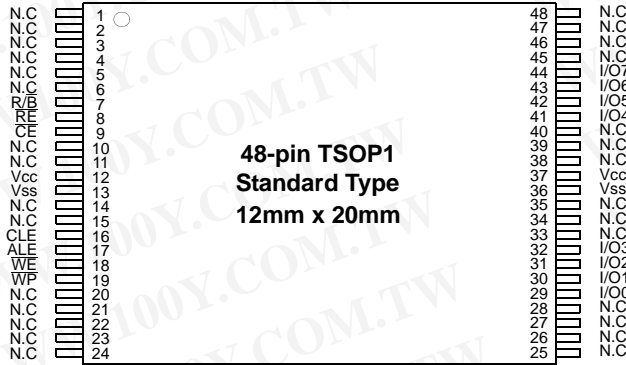
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**PIN CONFIGURATION (TSOP1)**

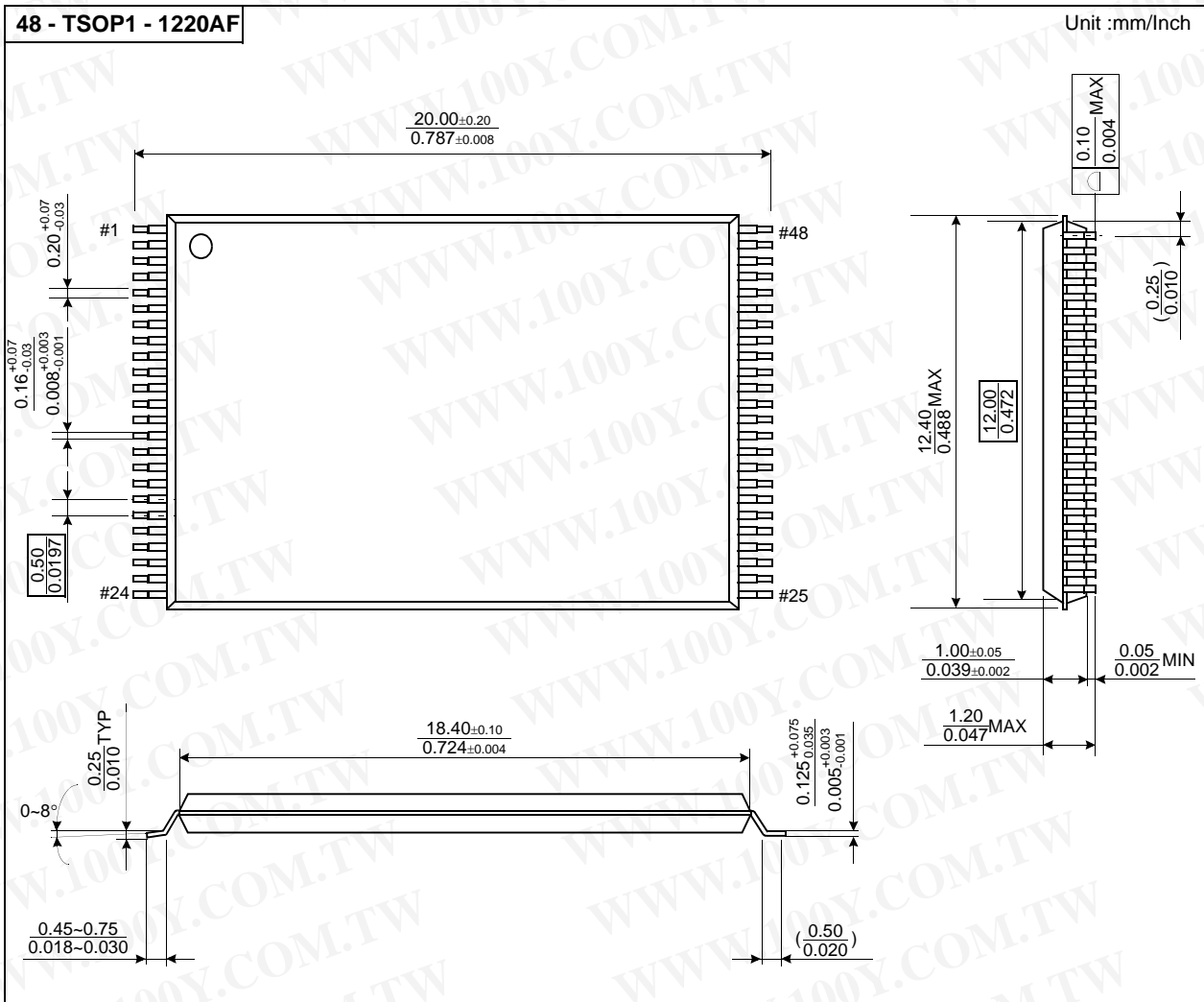
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**PACKAGE DIMENSIONS**

48-PIN LEAD/LEAD FREE PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(I)

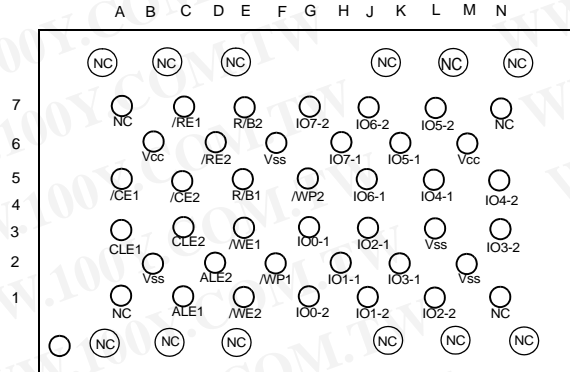




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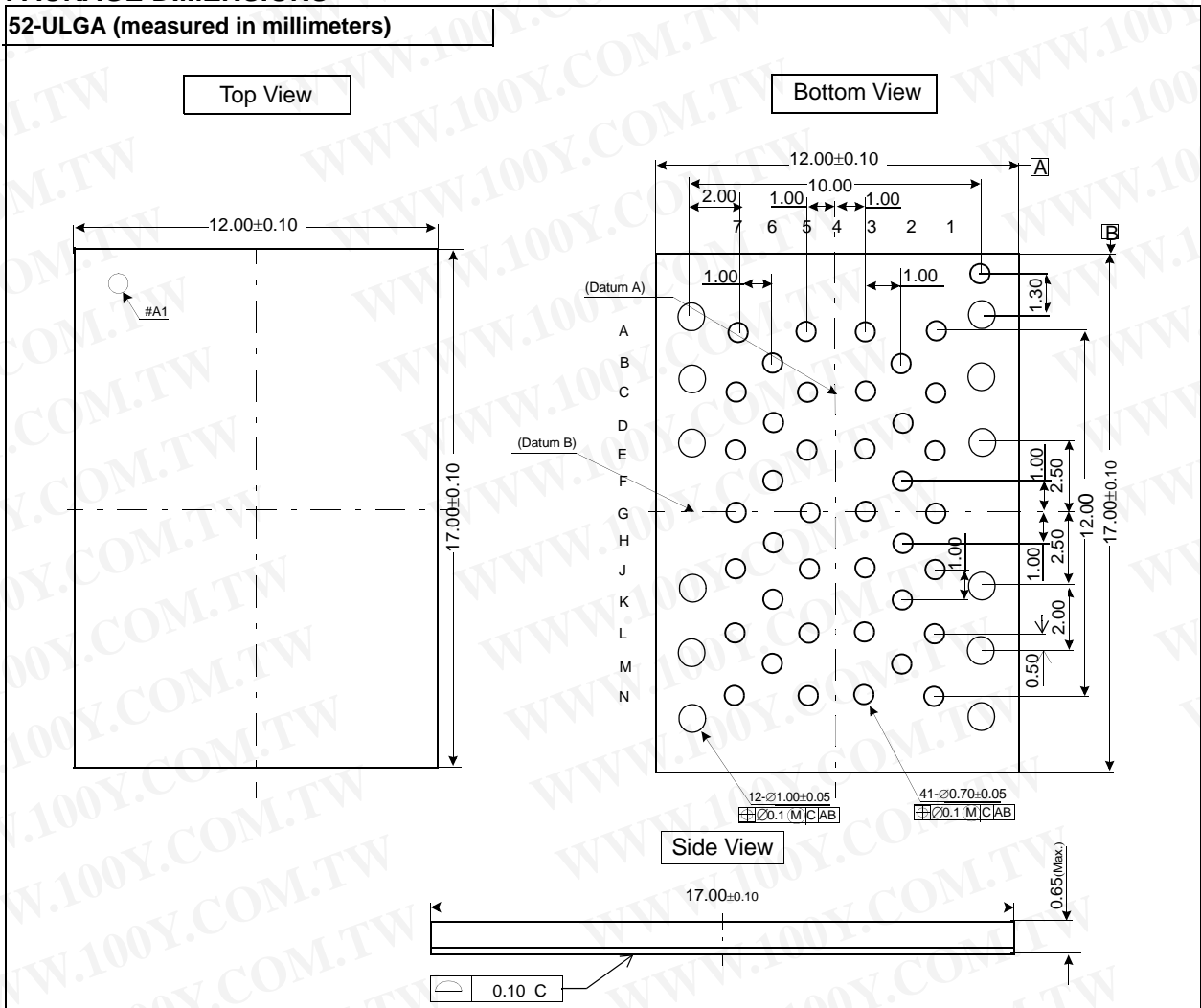
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**PACKAGE DIMENSIONS**

**52-ULGA (measured in millimeters)**



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**PIN DESCRIPTION**

| Pin Name                            | Pin Function  |
|-------------------------------------|---|
| I/O <sub>0</sub> ~ I/O <sub>7</sub> | <b>DATA INPUTS/OUTPUTS</b><br>The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.   |
| CLE                                 | <b>COMMAND LATCH ENABLE</b><br>The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the WE signal.  |
| ALE                                 | <b>ADDRESS LATCH ENABLE</b><br>The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of WE with ALE high.  |
| $\overline{\text{CE}}$              | <b>CHIP ENABLE</b><br>The $\overline{\text{CE}}$ input is the device selection control. When the device is in the Busy state, $\overline{\text{CE}}$ high is ignored, and the device does not return to standby mode in program or erase operation. Regarding $\overline{\text{CE}}$ control during read operation, refer to 'Page read' section of Device operation. |
| $\overline{\text{RE}}$              | <b>READ ENABLE</b><br>The $\overline{\text{RE}}$ input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of $\overline{\text{RE}}$ which also increments the internal column address counter by one.  |
| $\overline{\text{WE}}$              | <b>WRITE ENABLE</b><br>The $\overline{\text{WE}}$ input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the WE pulse.   |
| $\overline{\text{WP}}$              | <b>WRITE PROTECT</b><br>The $\overline{\text{WP}}$ pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the $\overline{\text{WP}}$ pin is active low.  |
| R/B                                 | <b>READY/BUSY OUTPUT</b><br>The R/B output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.                   |
| Vcc                                 | <b>POWER</b><br>Vcc is the power supply for device.   |
| Vss                                 | <b>GROUND</b>   |
| N.C                                 | <b>NO CONNECTION</b><br>Lead is not internally connected.   |

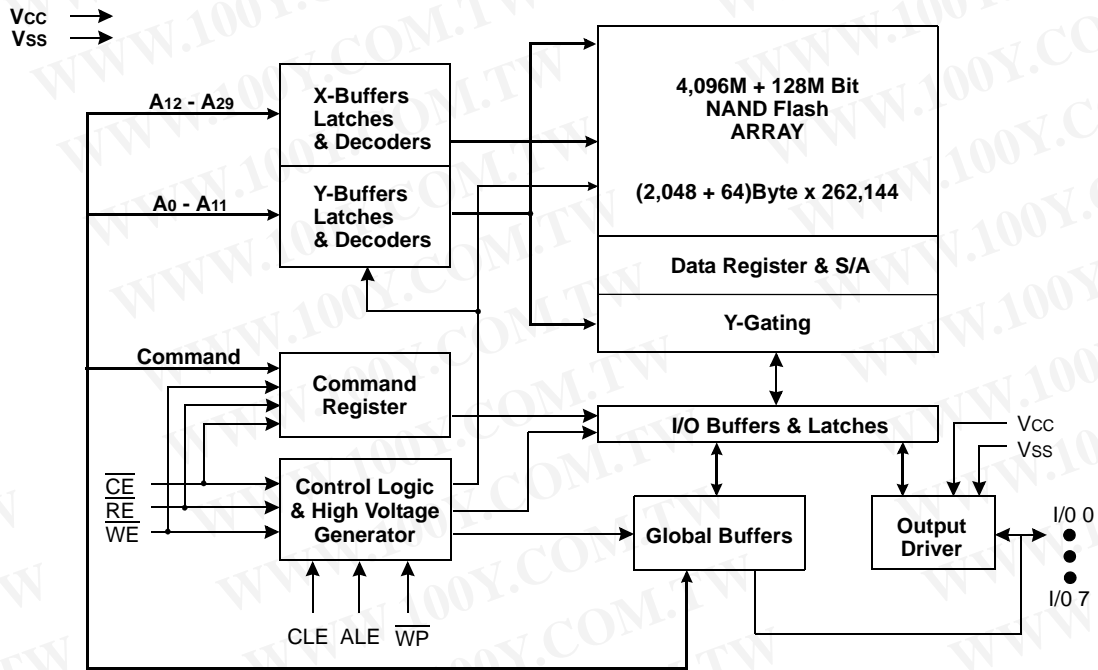
**NOTE** : Connect all Vcc and Vss pins of each device to common power supply outputs.  
Do not leave Vcc or Vss disconnected.

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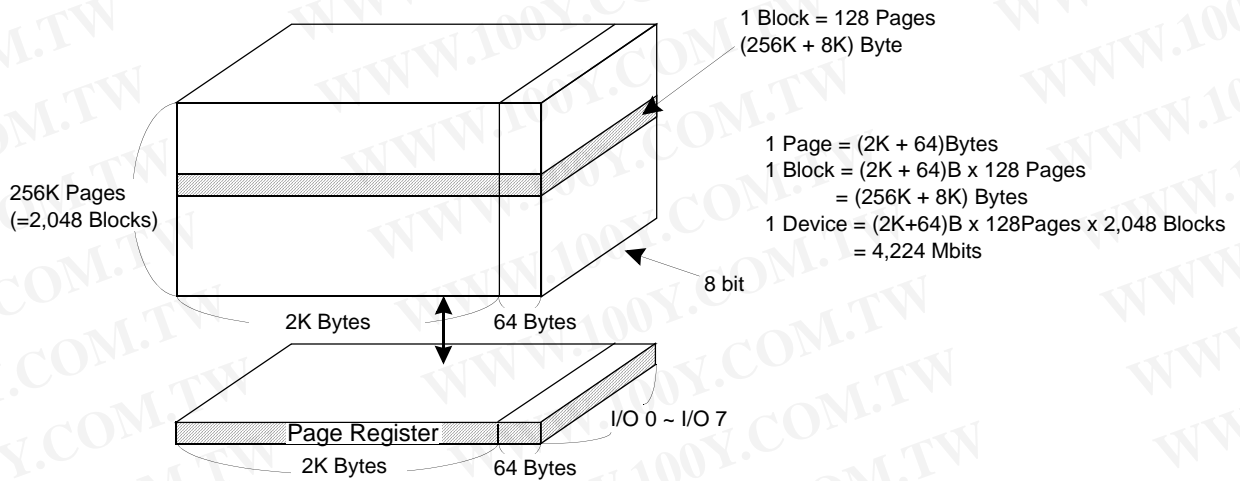
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**Figure 1-1. K9G4G08X0A Functional Block Diagram**



**Figure 2-1. K9G4G08X0A Array Organization**



|           | I/O 0           | I/O 1           | I/O 2           | I/O 3           | I/O 4           | I/O 5           | I/O 6           | I/O 7           |
|-----------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| 1st Cycle | A <sub>0</sub>  | A <sub>1</sub>  | A <sub>2</sub>  | A <sub>3</sub>  | A <sub>4</sub>  | A <sub>5</sub>  | A <sub>6</sub>  | A <sub>7</sub>  |
| 2nd Cycle | A <sub>8</sub>  | A <sub>9</sub>  | A <sub>10</sub> | A <sub>11</sub> | *L              | *L              | *L              | *L              |
| 3rd Cycle | A <sub>12</sub> | A <sub>13</sub> | A <sub>14</sub> | A <sub>15</sub> | A <sub>16</sub> | A <sub>17</sub> | A <sub>18</sub> | A <sub>19</sub> |
| 4th Cycle | A <sub>20</sub> | A <sub>21</sub> | A <sub>22</sub> | A <sub>23</sub> | A <sub>24</sub> | A <sub>25</sub> | A <sub>26</sub> | A <sub>27</sub> |
| 5th Cycle | A <sub>28</sub> | A <sub>29</sub> | *L              | *L              | *L              | *L              | *L              | *L              |

Column Address  
 Column Address  
 Row Address  
 Row Address  
 Row Address

NOTE : Column Address : Starting Address of the Register.

\* L must be set to "Low".

\* The device ignores any additional input of address cycles than required.

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## Preliminary FLASH MEMORY

### Product Introduction

The K9G4G08X0A is a 4,224Mbit(4,429,185,024bit) memory organized as 262,144 rows(pages) by 2,112x8 columns. Spare 64 columns are located from column address of 2,048~2,111. A 2,112-byte data register is connected to memory cell arrays for accommodating data transfer between the I/O buffers and memory cells during page read and page program operations. The memory array is made up of 32 cells that are serially connected to form a NAND structure. Each of the 32 cells resides in a different page. A block consists of two NAND structured strings. A NAND structure consists of 32 cells. A cell has 2-bit data. Total 1,081,344 NAND cells reside in a block. The program and read operations are executed on a page basis, while the erase operation is executed on a block basis. The memory array consists of 2,048 separately erasable 256K-byte blocks. It indicates that the bit by bit erase operation is prohibited on the K9G4G08X0A.

The K9G4G08X0A has addresses multiplexed into 8 I/Os. This scheme dramatically reduces pin counts and allows system upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through I/O's by bringing  $\overline{WE}$  to low while  $\overline{CE}$  is low. Those are latched on the rising edge of  $\overline{WE}$ . Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the I/O pins. Some commands require one bus cycle. For example, Reset Command, Status Read Command, etc require just one cycle bus. Some other commands, like page read and block erase and page program, require two cycles: one cycle for setup and the other cycle for execution. The 528M-byte physical space requires 30 addresses, thereby requiring five cycles for addressing : 2 cycles of column address, 3 cycles of row address, in that order. Page Read and Page Program need the same five address cycles following the required command input. In Block Erase operation, however, only three row address cycles are used. Device operations are selected by writing specific commands into the command register. Table 1 defines the specific commands of the K9G4G08X0A.

**Table 1. Command Sets**

| Function                                    | 1st Cycle  | 2nd Cycle  | Acceptable Command during Busy |
|---|------------|------------|--------------------------------|
| Read  | 00h        | 30h        |                                |
| Two-Plane Read                              | 60h----60h | 30h        |                                |
| Read ID                                     | 90h        | -          |                                |
| Reset                                       | FFh        | -          | O                              |
| Page Program                                | 80h        | 10h        |                                |
| Two-Plane Page Program <sup>(2)</sup>       | 80h----11h | 81h----10h |                                |
| Block Erase                                 | 60h        | D0h        |                                |
| Two-Plane Block Erase                       | 60h----60h | D0h        |                                |
| Random Data Input <sup>(1)</sup>            | 85h        | -          |                                |
| Random Data Output <sup>(1)</sup>           | 05h        | E0h        |                                |
| Two Plane Random Data Output <sup>(3)</sup> | 00h----05h | E0h        |                                |
| Read Status 1                               | 70h        | -          | O                              |
| Read Status 2                               | F1h        | -          | O                              |

**NOTE** : 1. Random Data Input/Output can be executed in a page.

2. Any command between 11h and 81h is prohibited except 70h/F1h and FFh.

3. Two-Plane Random Data Output must be used after Two-Plane Read operation.

**Caution** : Any undefined command inputs are prohibited except for above command set of Table 1.

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**ABSOLUTE MAXIMUM RATINGS**

| Parameter                          |                 | Symbol | Rating                  | Unit |
|------------------------------------|-----------------|--------|-------------------------|------|
| Voltage on any pin relative to Vss |                 | VCC    | -0.6 to + 4.6           | V    |
|                                    |                 | VIN    | -0.6 to + 4.6           |      |
|                                    |                 | VIO    | -0.6 to VCC+0.3 (<4.6V) |      |
| Temperature Under Bias             | K9XXG08XXA-XCB0 | TBIAS  | -10 to +125             | °C   |
|                                    | K9XXG08XXA-XIB0 |        | -40 to +125             |      |
| Storage Temperature                | K9XXG08XXA-XCB0 | TSTG   | -65 to +150             | °C   |
|                                    | K9XXG08XXA-XIB0 |        |                         |      |
| Short Circuit Current              |                 | Ios    | 5                       | mA   |

**NOTE :**

- Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns. Maximum DC voltage on input/output pins is VCC+0.3V which, during transitions, may overshoot to VCC+2.0V for periods <20ns.
- Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**RECOMMENDED OPERATING CONDITIONS**

(Voltage reference to GND, K9XXG08XXA-XCB0 :TA=0 to 70°C, K9XXG08XXA-XIB0:TA=-40 to 85°C)

| Parameter      | Symbol | K9G4G08B0A(2.7V) |      |     | K9G4G08U0A(3.3V) |      |     | Unit |
|----------------|--------|------------------|------|-----|------------------|------|-----|------|
|                |        | Min              | Typ. | Max | Min              | Typ. | Max |      |
| Supply Voltage | VCC    | 2.5              | 2.7  | 2.9 | 2.7              | 3.3  | 3.6 | V    |
| Supply Voltage | VSS    | 0                | 0    | 0   | 0                | 0    | 0   | V    |

**DC AND OPERATING CHARACTERISTICS**(Recommended operating conditions otherwise noted.)

| Parameter                     |                              | Symbol   | Test Conditions  | K9G4G08X0A  |     |             |      |     |             | Unit |
|-------------------------------|------------------------------|----------|--|-------------|-----|-------------|------|-----|-------------|------|
|                               |                              |          |  | 2.7V        |     |             | 3.3V |     |             |      |
|                               |                              |          |  | Min         | Typ | Max         | Min  | Typ | Max         |      |
| Operating Current             | Page Read with Serial Access | Icc1     | tRC=50ns, $\overline{CE}=V_{IL}$<br>IOUT=0mA                             | -           | 15  | 30          | -    | 15  | 30          | mA   |
|                               | Program                      | Icc2     | -  | -           | 15  | 30          | -    | 15  | 30          |      |
|                               | Erase                        | Icc3     | -  | -           | 15  | 30          | -    | 15  | 30          |      |
| Stand-by Current(TTL)         |                              | ISB1     | $\overline{CE}=V_{IH}$ , $\overline{WP}=\overline{PRE}=0V/V_{CC}$        | -           | -   | 1           | -    | -   | 1           | µA   |
| Stand-by Current(CMOS)        |                              | ISB2     | $\overline{CE}=V_{CC}-0.2$ ,<br>$\overline{WP}=\overline{PRE}=0V/V_{CC}$ | -           | 10  | 50          | -    | 10  | 50          |      |
| Input Leakage Current         |                              | ILI      | VIN=0 to VCC(max)  | -           | -   | ±10         | -    | -   | ±10         | µA   |
| Output Leakage Current        |                              | ILO      | VOUT=0 to VCC(max)   | -           | -   | ±10         | -    | -   | ±10         |      |
| Input High Voltage            |                              | VIH*     | -  | VCC<br>-0.4 | -   | VCC<br>+0.3 | 2.0  | -   | VCC<br>+0.3 | V    |
| Input Low Voltage, All inputs |                              | VIL*     | -  | -0.3        | -   | 0.5         | -0.3 | -   | 0.8         |      |
| Output High Voltage Level     |                              | VOH      | K9G4G08B0A :IOH=-100µA<br>K9G4G08U0A :IOH=-400µA                         | VCC<br>-0.4 | -   | -           | 2.4  | -   | -           |      |
| Output Low Voltage Level      |                              | VOL      | K9G4G08B0A :IOL=100µA<br>K9G4G08U0A :IOL=2.1mA                           | -           | -   | 0.4         | -    | -   | 0.4         |      |
| Output Low Current(R/B)       |                              | IOL(R/B) | K9G4G08B0A :VOL=0.1V<br>K9G4G08U0A :VOL=0.4V                             | 3           | 4   | -           | 8    | 10  | -           | mA   |

**NOTE :**

- VIL can undershoot to -0.4V and VIH can overshoot to VCC + 0.4V for durations of 20 ns or less.
- Typical value is measured at VCC=2.7V/3.3V, TA=25°C. Not 100% tested.
- The typical value of the K9L8G08U1A's ISB2 is 20µA and the maximum value is 100µA.

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**VALID BLOCK**

| Parameter   | Symbol | Min   | Typ. | Max   | Unit   |
|-------------|--------|-------|------|-------|--------|
| K9G4G08X0A  | NvB    | 1,998 | -    | 2,048 | Blocks |
| K9L8G08U1A* | NvB    | 3,996 | -    | 4,096 | Blocks |

**NOTE :**

- The device may include initial invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for appropriate management of initial invalid blocks.
  - The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the time of shipment.
  - The number of valid block is on the basis of single plane operations, and this may be decreased with two plane operations.
- \* : Each K9G4G08U0A chip in the K9L8G08U1A has Maximun 50 invalid blocks.

**AC TEST CONDITION**

(K9XXG08XXA-XCB0 :TA=0 to 70°C, K9XXG08XXA-XIB0:TA=-40 to 85°C,  
 K9XXG08BXA: Vcc=2.5V~2.9V, K9XXG08UXA: Vcc=2.7V~3.6V unless otherwise)

| Parameter                      | K9G4G08B0A             | K9XXG08UXA             |
|--------------------------------|------------------------|------------------------|
| Input Pulse Levels             | 0V to Vcc              | 0V to Vcc              |
| Input Rise and Fall Times      | 5ns                    | 5ns                    |
| Input and Output Timing Levels | Vcc/2                  | Vcc/2                  |
| Output Load                    | 1 TTL GATE and CL=30pF | 1 TTL GATE and CL=50pF |

**CAPACITANCE**(TA=25°C, VCC=2.7V/3.3V, f=1.0MHz)

| Item                     | Symbol           | Test Condition      | Min | Max | Unit |
|--------------------------|------------------|---------------------|-----|-----|------|
| Input/Output Capacitance | C <sub>I/O</sub> | V <sub>IL</sub> =0V | -   | 10  | pF   |
| Input Capacitance        | C <sub>IN</sub>  | V <sub>IN</sub> =0V | -   | 10  | pF   |

**NOTE :** Capacitance is periodically sampled and not 100% tested.

**MODE SELECTION**

| CLE | ALE              | CE | WE | RE | WP                    | Mode                 |                       |
|-----|------------------|----|----|----|-----------------------|----------------------|-----------------------|
| H   | L                | L  |    | H  | X                     | Read Mode            | Command Input         |
| L   | H                | L  |    | H  | X                     |                      | Address Input(5clock) |
| H   | L                | L  |    | H  | H                     | Write Mode           | Command Input         |
| L   | H                | L  |    | H  | H                     |                      | Address Input(5clock) |
| L   | L                | L  |    | H  | H                     | Data Input           |                       |
| L   | L                | L  | H  |    | X                     | Data Output          |                       |
| X   | X                | X  | X  | H  | X                     | During Read(Busy)    |                       |
| X   | X                | X  | X  | X  | H                     | During Program(Busy) |                       |
| X   | X                | X  | X  | X  | H                     | During Erase(Busy)   |                       |
| X   | X <sup>(1)</sup> | X  | X  | X  | L                     | Write Protect        |                       |
| X   | X                | H  | X  | X  | 0V/Vcc <sup>(2)</sup> | Stand-by             |                       |

**NOTE :** 1. X can be V<sub>IL</sub> or V<sub>IH</sub>.

2. WP should be biased to CMOS high or CMOS low for standby.

**K9L8G08U1A**  
**K9G4G08U0A K9G4G08B0A**
**Preliminary**  
**FLASH MEMORY**
**Program / Erase Characteristics**

| Parameter   | Symbol | Min | Typ | Max | Unit  |
|---|--------|-----|-----|-----|-------|
| Program Time                                      | tPROG  | -   | 0.8 | 3   | ms    |
| Dummy Busy Time for Multi Plane Program           | tdBSY  | -   | 0.5 | 1   | μs    |
| Number of Partial Program Cycles in the Same Page | Nop    | -   | -   | 1   | cycle |
| Block Erase Time                                  | tBERS  | -   | 1.5 | 10  | ms    |

**NOTE**

1. Typical value is measured at Vcc=3.3V, TA=25°C. Not 100% tested.
2. Typical Program time is defined as the time within which more than 50% of the whole pages are programmed at 3.3V Vcc and 25°C temperature.
3. Within a same block, program time(tPROG) of page group A is faster than that of page group B. Typical tPROG is the average program time of the page group A and B(Table 2).

Page Group A: Page 0, 1, 2, 3, 6, 7, 10, 11, ..., 110, 111, 114, 115, 118, 119, 122, 123

Page Group B: Page 4, 5, 8, 9, 12, 13, 16, 17, ..., 116, 117, 120, 121, 124, 125, 126, 127

**AC Timing Characteristics for Command / Address / Data Input**

| Parameter                             | Symbol              | Min                | Max | Unit |
|---------------------------------------|---------------------|--------------------|-----|------|
| CLE Setup Time                        | tCLS <sup>(1)</sup> | 15                 | -   | ns   |
| CLE Hold Time                         | tCLH                | 5                  | -   | ns   |
| $\overline{\text{CE}}$ Setup Time     | tCS <sup>(1)</sup>  | 20                 | -   | ns   |
| $\overline{\text{CE}}$ Hold Time      | tCH                 | 5                  | -   | ns   |
| $\overline{\text{WE}}$ Pulse Width    | tWP                 | 15                 | -   | ns   |
| ALE Setup Time                        | tALS <sup>(1)</sup> | 15                 | -   | ns   |
| ALE Hold Time                         | tALH                | 5                  | -   | ns   |
| Data Setup Time                       | tDS <sup>(1)</sup>  | 15                 | -   | ns   |
| Data Hold Time                        | tDH                 | 5                  | -   | ns   |
| Write Cycle Time                      | tWC                 | 30                 | -   | ns   |
| $\overline{\text{WE}}$ High Hold Time | tWH                 | 10                 | -   | ns   |
| Address to Data Loading Time          | tADL <sup>(2)</sup> | 100 <sup>(2)</sup> | -   | ns   |

**NOTES** : 1. The transition of the corresponding control pins must occur only once while  $\overline{\text{WE}}$  is held low.

2. tADL is the time from the  $\overline{\text{WE}}$  rising edge of final address cycle to the  $\overline{\text{WE}}$  rising edge of first data cycle.

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**K9L8G08U1A**  
**K9G4G08U0A K9G4G08B0A**
**Preliminary**  
**FLASH MEMORY**
**AC Characteristics for Operation**

| Parameter                                     | Symbol            | Min | Max                     | Unit |
|---|-------------------|-----|-------------------------|------|
| Data Transfer from Cell to Register           | t <sub>R</sub>    | -   | 60                      | μs   |
| ALE to $\overline{RE}$ Delay                  | t <sub>AR</sub>   | 10  | -                       | ns   |
| CLE to $\overline{RE}$ Delay                  | t <sub>CLR</sub>  | 10  | -                       | ns   |
| Ready to $\overline{RE}$ Low                  | t <sub>RR</sub>   | 20  | -                       | ns   |
| $\overline{RE}$ Pulse Width                   | t <sub>RP</sub>   | 15  | -                       | ns   |
| $\overline{WE}$ High to Busy                  | t <sub>WB</sub>   | -   | 100                     | ns   |
| Read Cycle Time                               | t <sub>RC</sub>   | 30  | -                       | ns   |
| $\overline{RE}$ Access Time                   | t <sub>REA</sub>  | -   | 20                      | ns   |
| $\overline{CE}$ Access Time                   | t <sub>CEA</sub>  | -   | 25                      | ns   |
| $\overline{RE}$ High to Output Hi-Z           | t <sub>RHZ</sub>  | -   | 100                     | ns   |
| $\overline{CE}$ High to Output Hi-Z           | t <sub>CHZ</sub>  | -   | 30                      | ns   |
| $\overline{CE}$ High to ALE or CLE Don't Care | t <sub>CSD</sub>  | 10  | -                       | ns   |
| $\overline{RE}$ High to Output Hold           | t <sub>RHOH</sub> | 15  | -                       | ns   |
| $\overline{RE}$ Low to Output Hold            | t <sub>RLOH</sub> | 5   | -                       | ns   |
| $\overline{CE}$ High to Output Hold           | t <sub>COH</sub>  | 15  | -                       | ns   |
| $\overline{RE}$ High Hold Time                | t <sub>REH</sub>  | 10  | -                       | ns   |
| Output Hi-Z to $\overline{RE}$ Low            | t <sub>IR</sub>   | 0   | -                       | ns   |
| $\overline{RE}$ High to $\overline{WE}$ Low   | t <sub>RHW</sub>  | 100 | -                       | ns   |
| $\overline{WE}$ High to $\overline{RE}$ Low   | t <sub>WHR</sub>  | 60  | -                       | ns   |
| Device Resetting Time(Read/Program/Erase)     | t <sub>RST</sub>  | -   | 5/10/500 <sup>(1)</sup> | μs   |

NOTE: 1. If reset command(FFh) is written at Ready state, the device goes into Busy for maximum 5μs.

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# K9L8G08U1A K9G4G08U0A K9G4G08B0A

## Preliminary FLASH MEMORY

### NAND Flash Technical Notes

#### Initial Invalid Block(s)

Initial invalid blocks are defined as blocks that contain one or more initial invalid bits whose reliability is not guaranteed by Samsung. The information regarding the initial invalid block(s) is called the initial invalid block information. Devices with initial invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An initial invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the initial invalid block(s) via address mapping. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the time of shipment.

#### Identifying Initial Invalid Block(s)

All device locations are erased(FFh) except locations where the initial invalid block(s) information is written prior to shipping. The initial invalid block(s) status is defined by the 1st byte in the spare area. Samsung makes sure that the last page of every initial invalid block has non-FFh data at the column address of 2,048. The initial invalid block information is also erasable in most cases, and it is impossible to recover the information once it has been erased. Therefore, the system must be able to recognize the initial invalid block(s) based on the initial invalid block information and create the initial invalid block table via the following suggested flow chart(Figure 3). Any intentional erasure of the initial invalid block information is prohibited.

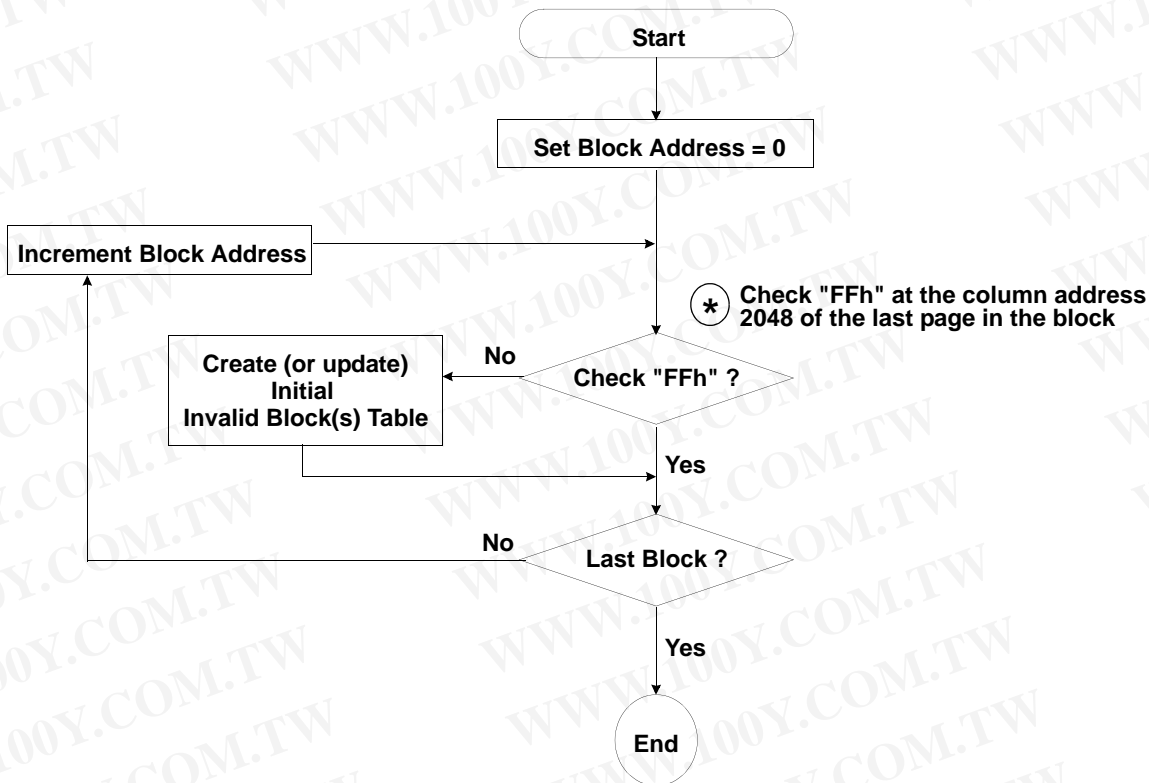


Figure 3. Flow chart to create initial invalid block table.

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**K9L8G08U1A  
K9G4G08U0A K9G4G08B0A**

**Preliminary  
FLASH MEMORY**

**NAND Flash Technical Notes (Continued)**

**Error in write or read operation**

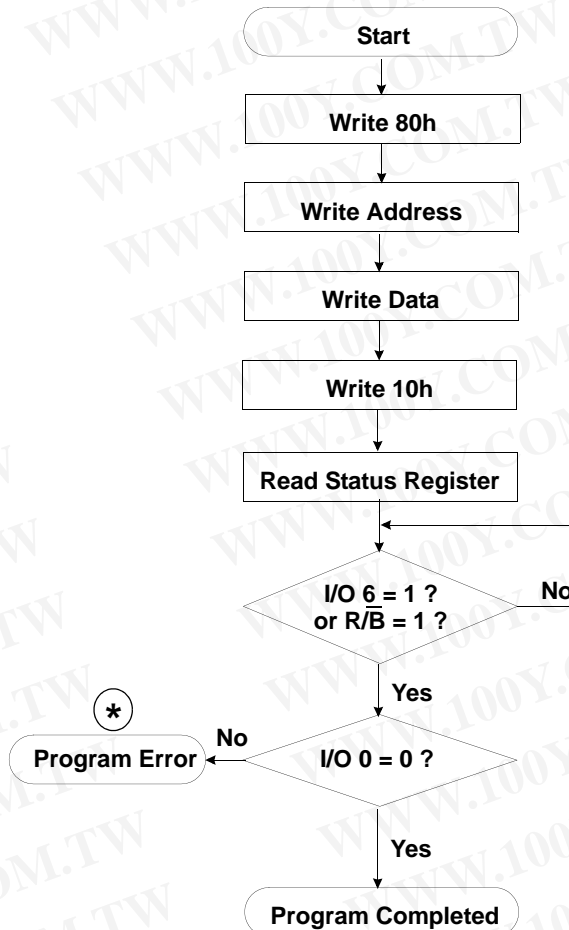
Within its life time, additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the actual data. Block replacement should be done upon erase or program error.

|       | Failure Mode           | Detection and Countermeasure sequence           |
|-------|------------------------|---|
| Write | Erase Failure          | Status Read after Erase --> Block Replacement   |
|       | Program Failure        | Status Read after Program --> Block Replacement |
| Read  | Up to Four Bit Failure | Verify ECC -> ECC Correction                    |

**ECC** : Error Correcting Code --> RS Code etc.  
Example) 4bit correction / 512-byte

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**Program Flow Chart**



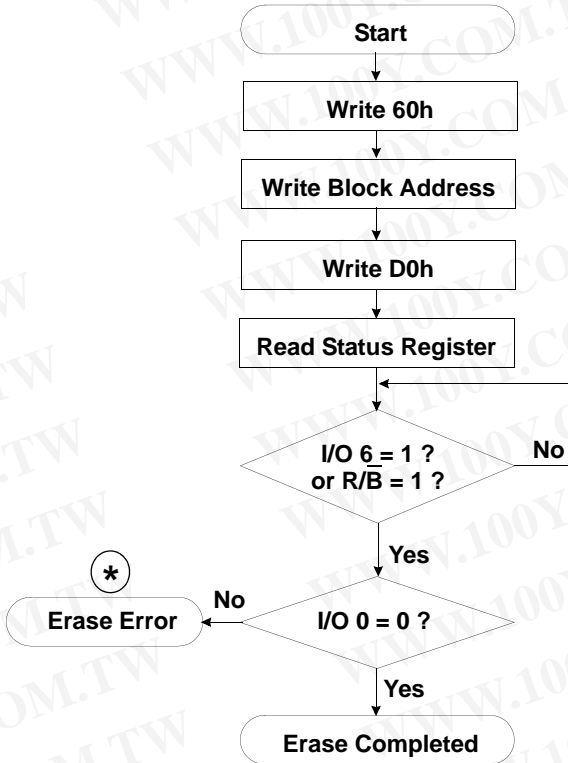
**\*** : If program operation results in an error, map out the block including the page in error and copy the target data to another block.

**K9L8G08U1A  
K9G4G08U0A K9G4G08B0A**

**Preliminary  
FLASH MEMORY**

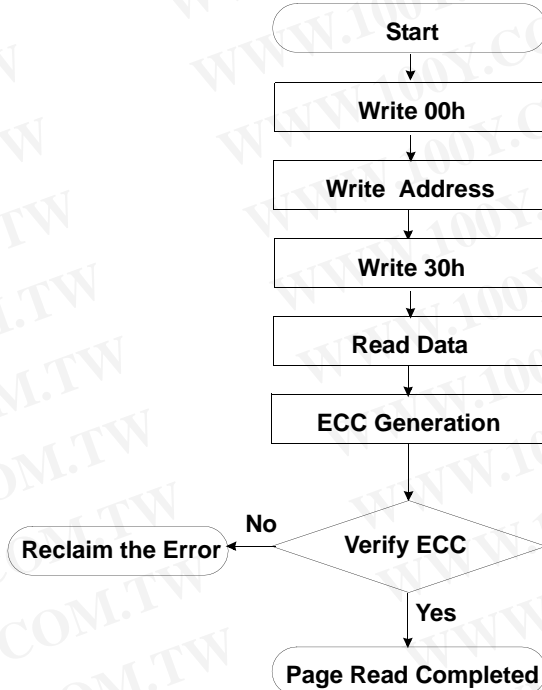
**NAND Flash Technical Notes (Continued)**

**Erase Flow Chart**

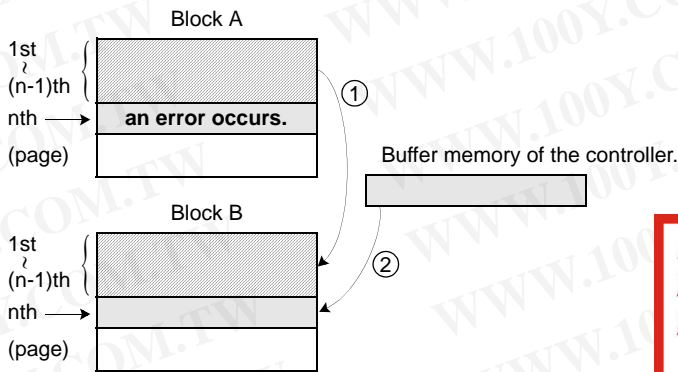


\* : If erase operation results in an error, map out the failing block and replace it with another block.

**Read Flow Chart**



**Block Replacement**



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- \* Step1  
When an error happens in the nth page of the Block 'A' during erase or program operation.
- \* Step2  
Copy the data in the 1st ~ (n-1)th page to the same location of another free block. (Block 'B')
- \* Step3  
Then, copy the nth page data of the Block 'A' in the buffer memory to the nth page of the Block 'B'.
- \* Step4  
Do not erase or program to Block 'A' by creating an 'invalid block' table or other appropriate scheme.

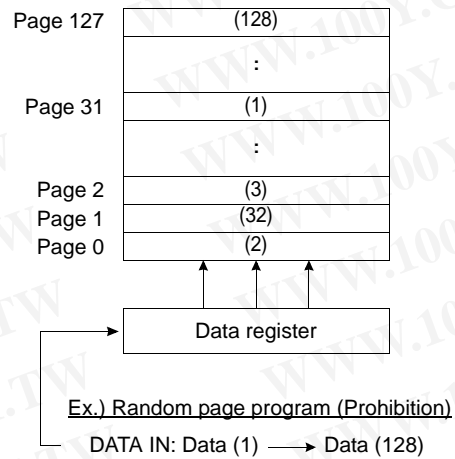
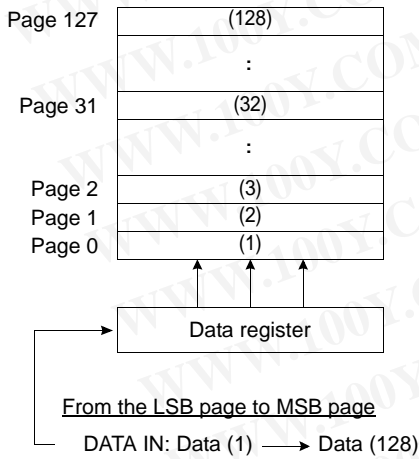
**K9L8G08U1A  
K9G4G08U0A K9G4G08B0A**

**Preliminary  
FLASH MEMORY**

**NAND Flash Technical Notes (Continued)**

**Addressing for program operation**

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) page of the block. Random page address programming is prohibited. In this case, the definition of LSB page is the LSB among the pages to be programmed. Therefore, LSB page doesn't need to be page 0.



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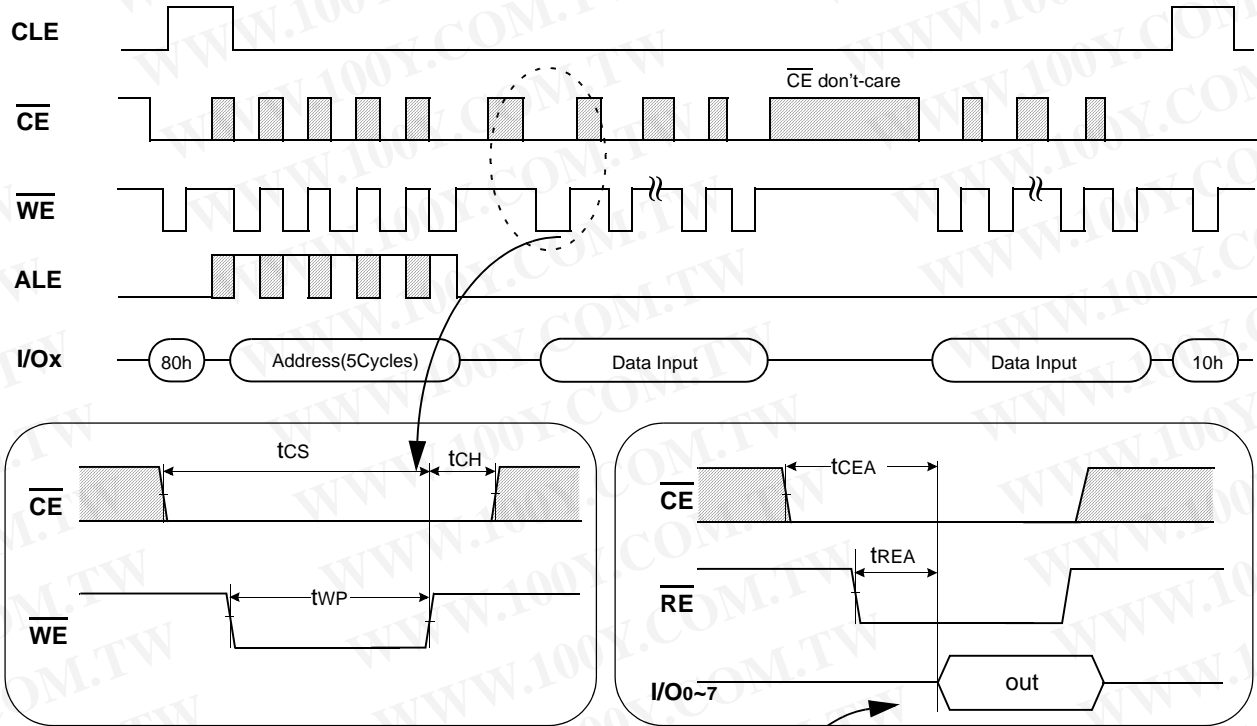
**K9L8G08U1A  
 K9G4G08U0A K9G4G08B0A**

**Preliminary  
 FLASH MEMORY**

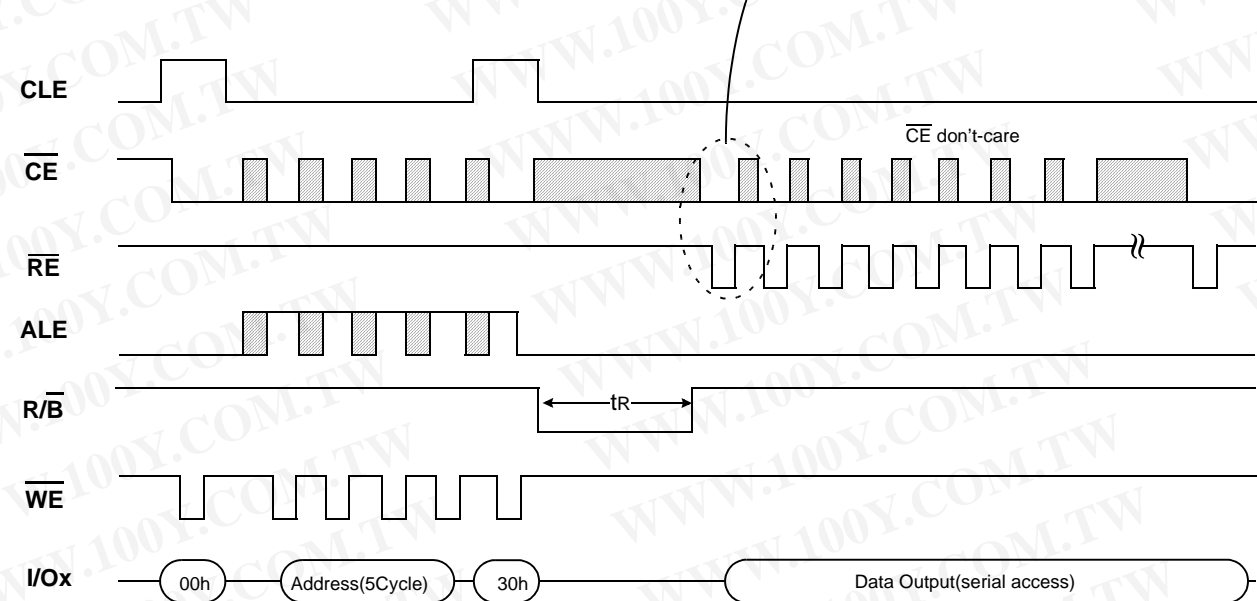
**System Interface Using  $\overline{CE}$  don't-care.**

For an easier system interface,  $\overline{CE}$  may be inactive during the data-loading or serial access as shown below. The internal 2,112byte data registers are utilized as separate buffers for this operation and the system design gets more flexible. In addition, for voice or audio applications which use slow cycle time on the order of  $\mu$ -seconds, de-activating  $\overline{CE}$  during the data-loading and serial access would provide significant savings in power consumption.

**Figure 4. Program Operation with  $\overline{CE}$  don't-care.**



**Figure 5. Read Operation with  $\overline{CE}$  don't-care.**



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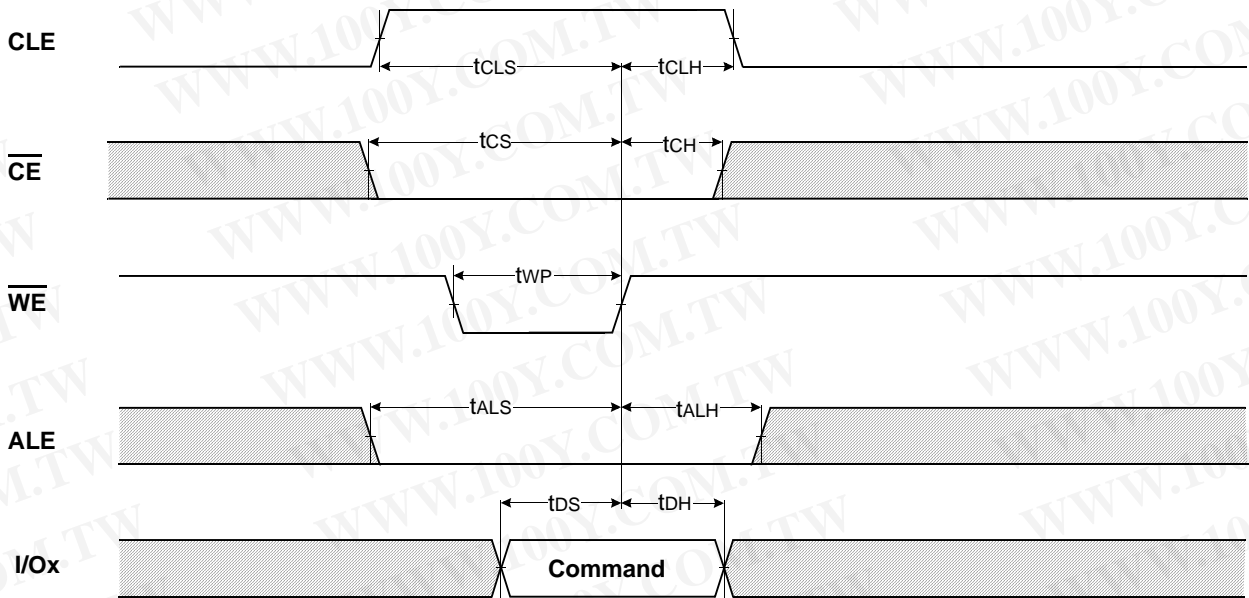
**K9L8G08U1A  
 K9G4G08U0A K9G4G08B0A**

**Preliminary  
 FLASH MEMORY**

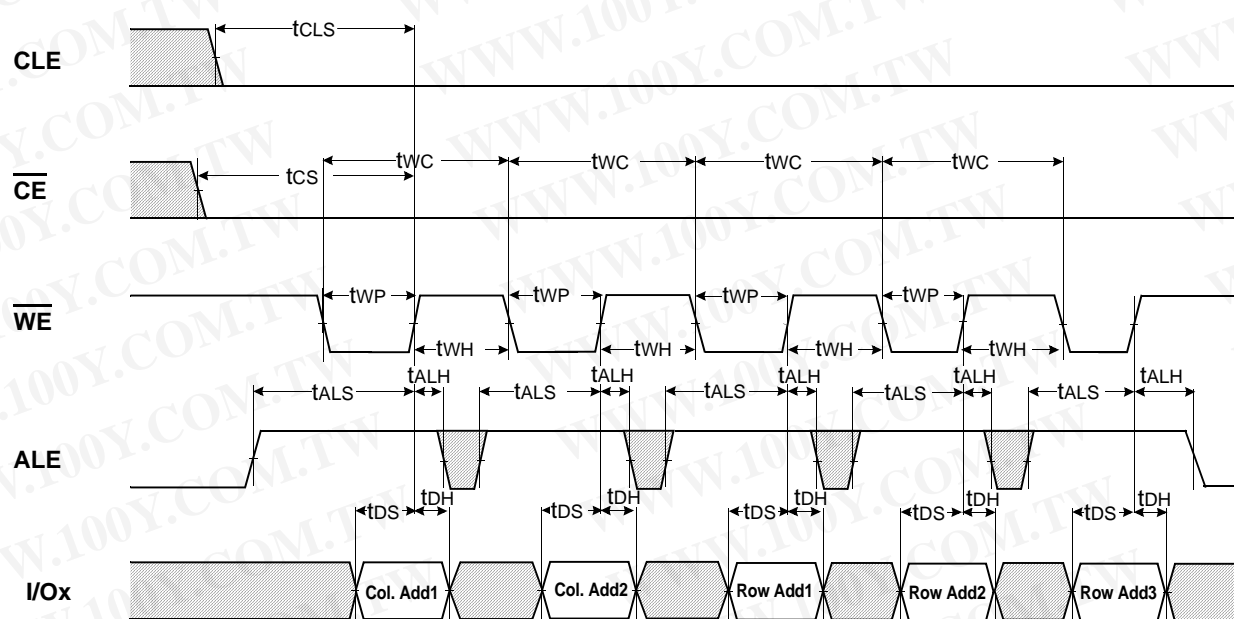
NOTE

| Device     | I/O           | DATA        | ADDRESS   |           |          |          |          |
|------------|---------------|-------------|-----------|-----------|----------|----------|----------|
|            | I/Ox          | Data In/Out | Col. Add1 | Col. Add2 | Row Add1 | Row Add2 | Row Add3 |
| K9G4G08X0A | I/O 0 ~ I/O 7 | ~2,112byte  | A0~A7     | A8~A11    | A12~A19  | A20~A27  | A28~A29  |

**Command Latch Cycle**



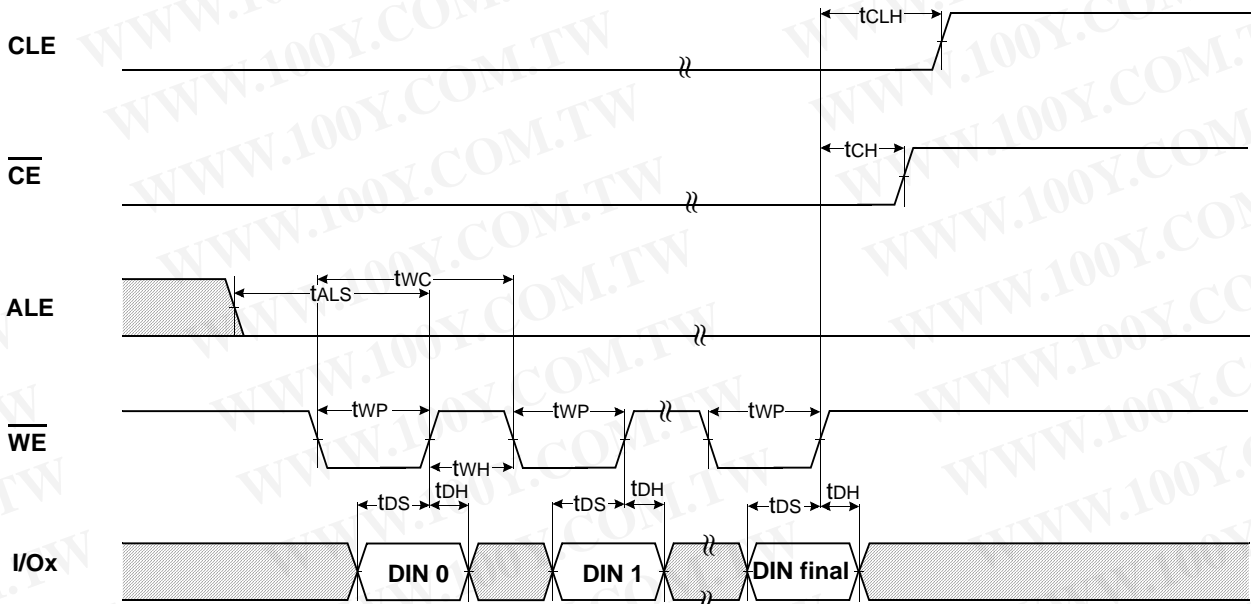
**Address Latch Cycle**



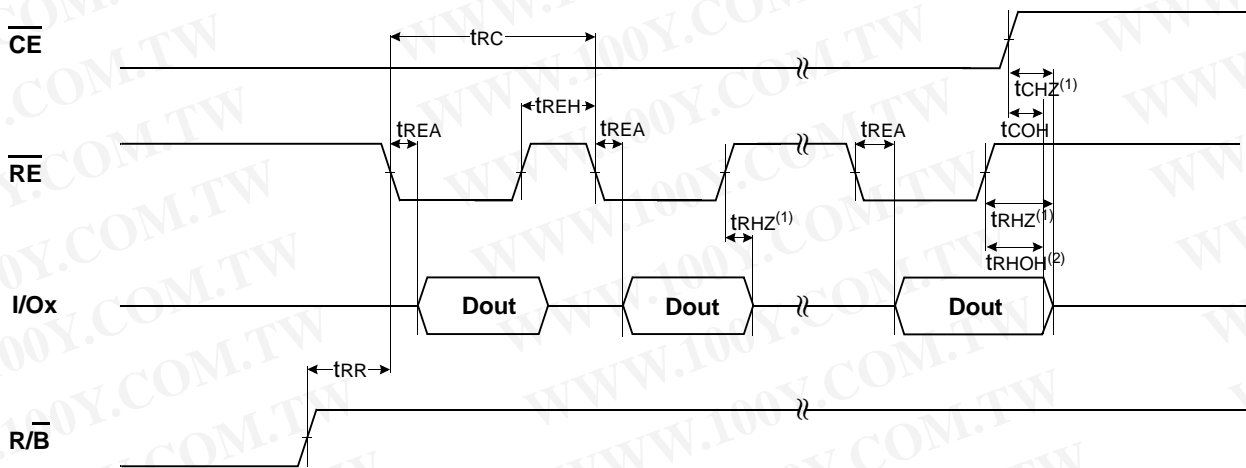
**K9L8G08U1A  
 K9G4G08U0A K9G4G08B0A**

**Preliminary  
 FLASH MEMORY**

**Input Data Latch Cycle**



**\* Serial Access Cycle after Read (CLE=L, WE=H, ALE=L)**

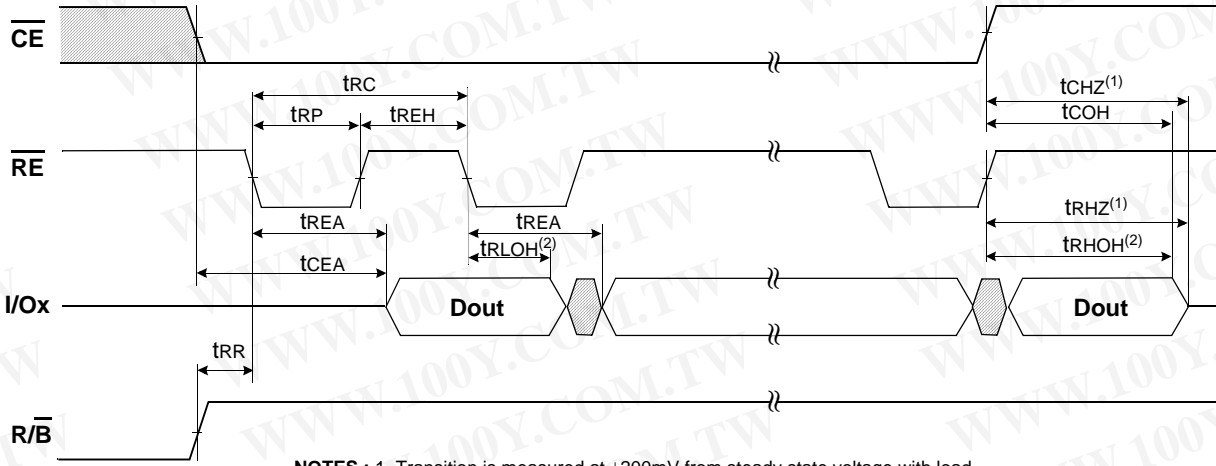


- NOTES : 1. Transition is measured at  $\pm 200\text{mV}$  from steady state voltage with load.  
 This parameter is sampled and not 100% tested.  
 2. tRHOH starts to be valid when frequency is lower than 20MHz.

**K9L8G08U1A  
 K9G4G08U0A K9G4G08B0A**

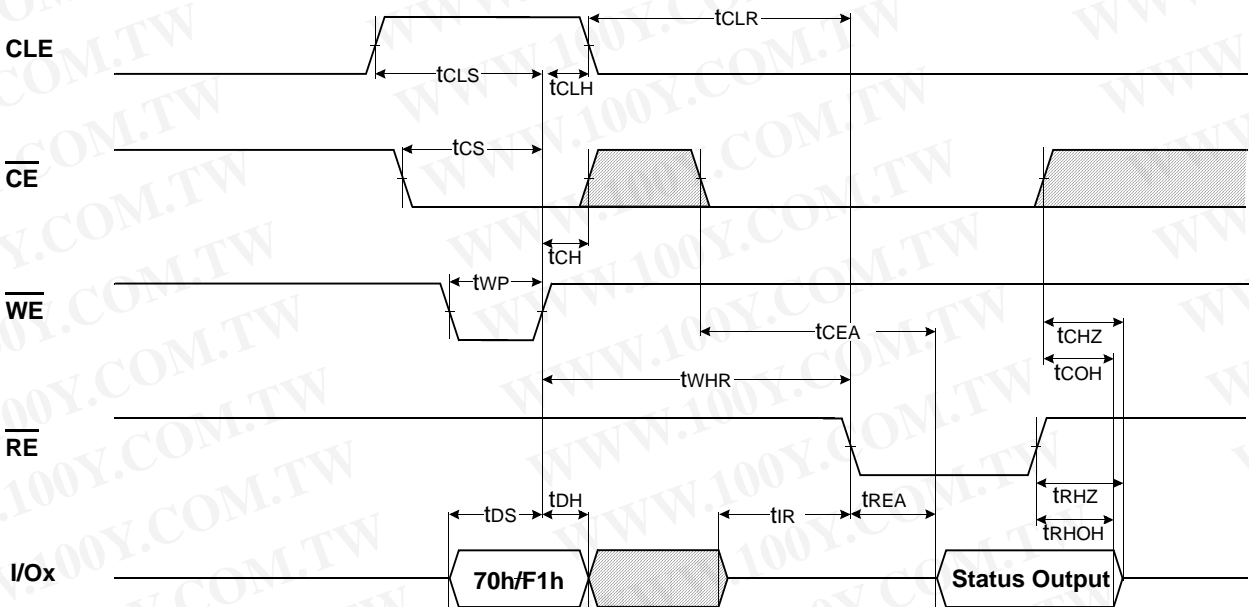
**Preliminary  
 FLASH MEMORY**

**Serial Access Cycle after Read(EDO Type, CLE=L,  $\overline{WE}$ =H, ALE=L)**



- NOTES :** 1. Transition is measured at  $\pm 200mV$  from steady state voltage with load. This parameter is sampled and not 100% tested.  
 2.  $t_{RLOH}$  is valid when frequency is higher than 20MHz.  $t_{RHOH}$  starts to be valid when frequency is lower than 20MHz.

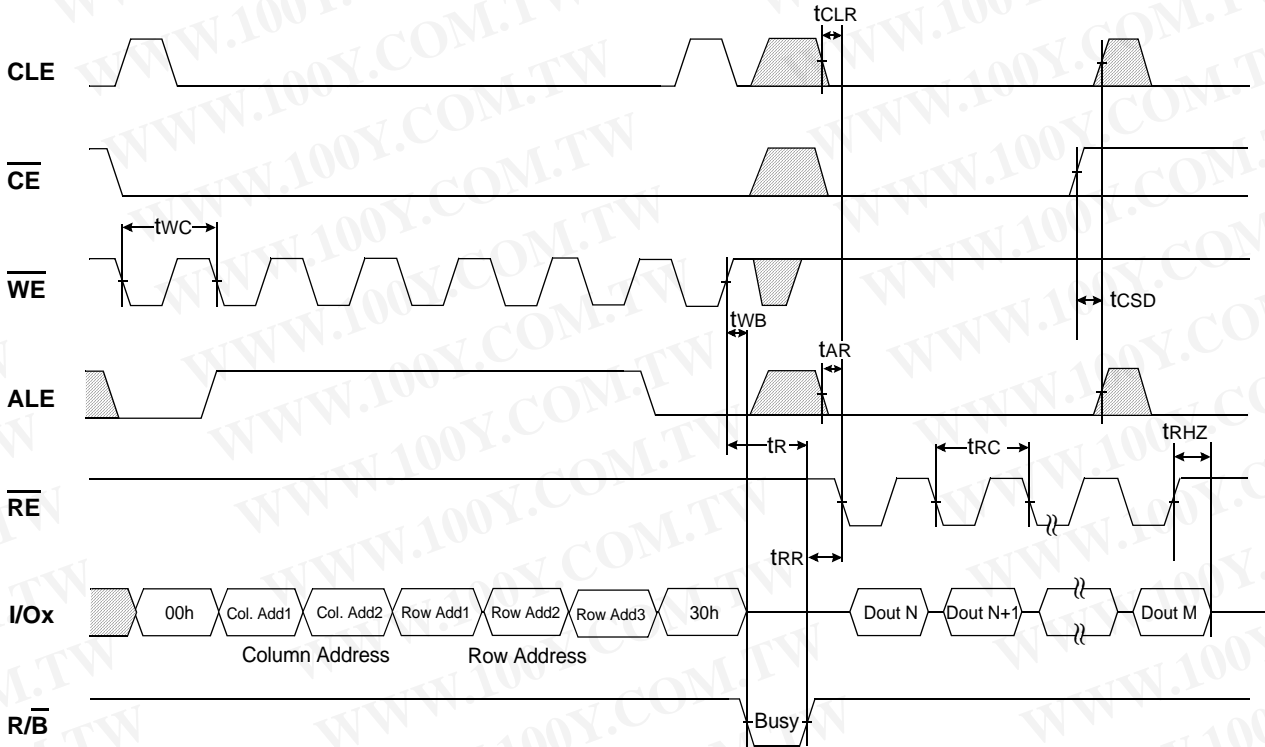
**Status Read Cycle**



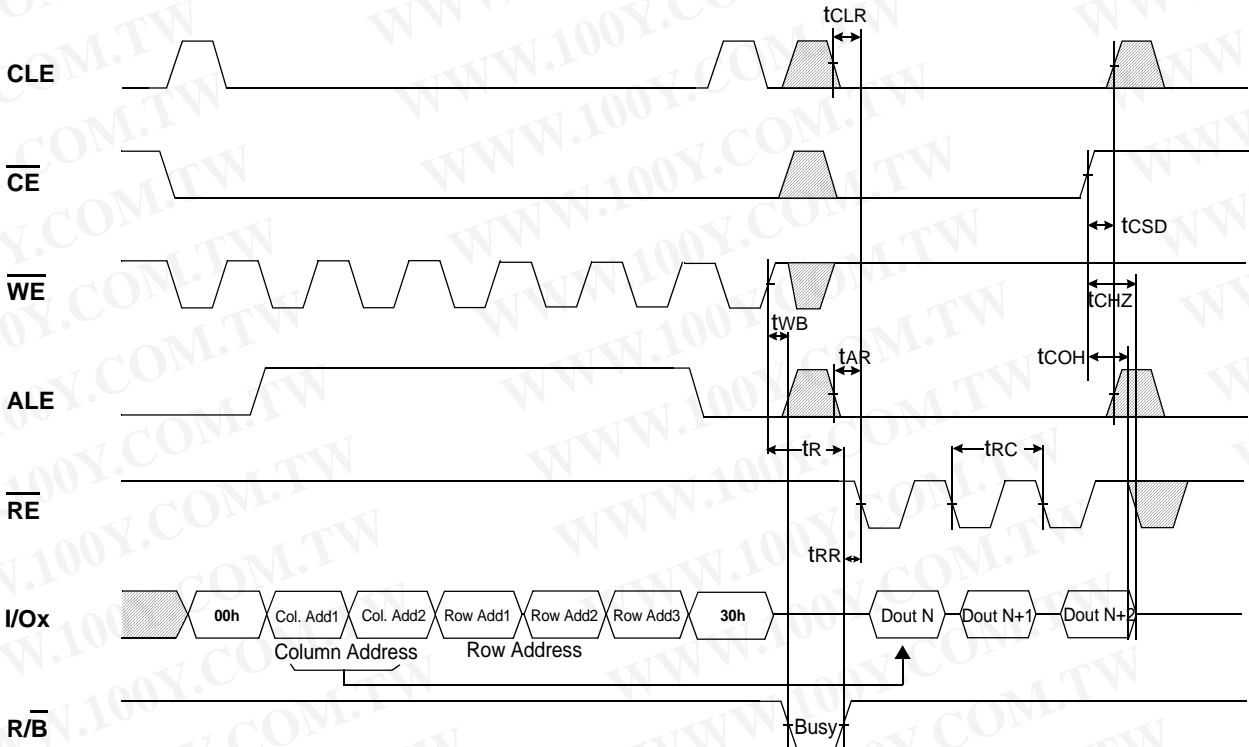
**Preliminary  
FLASH MEMORY**

**K9L8G08U1A  
K9G4G08U0A K9G4G08B0A**

**Read Operation**



**Read Operation(Intercepted by  $\overline{CE}$ )**

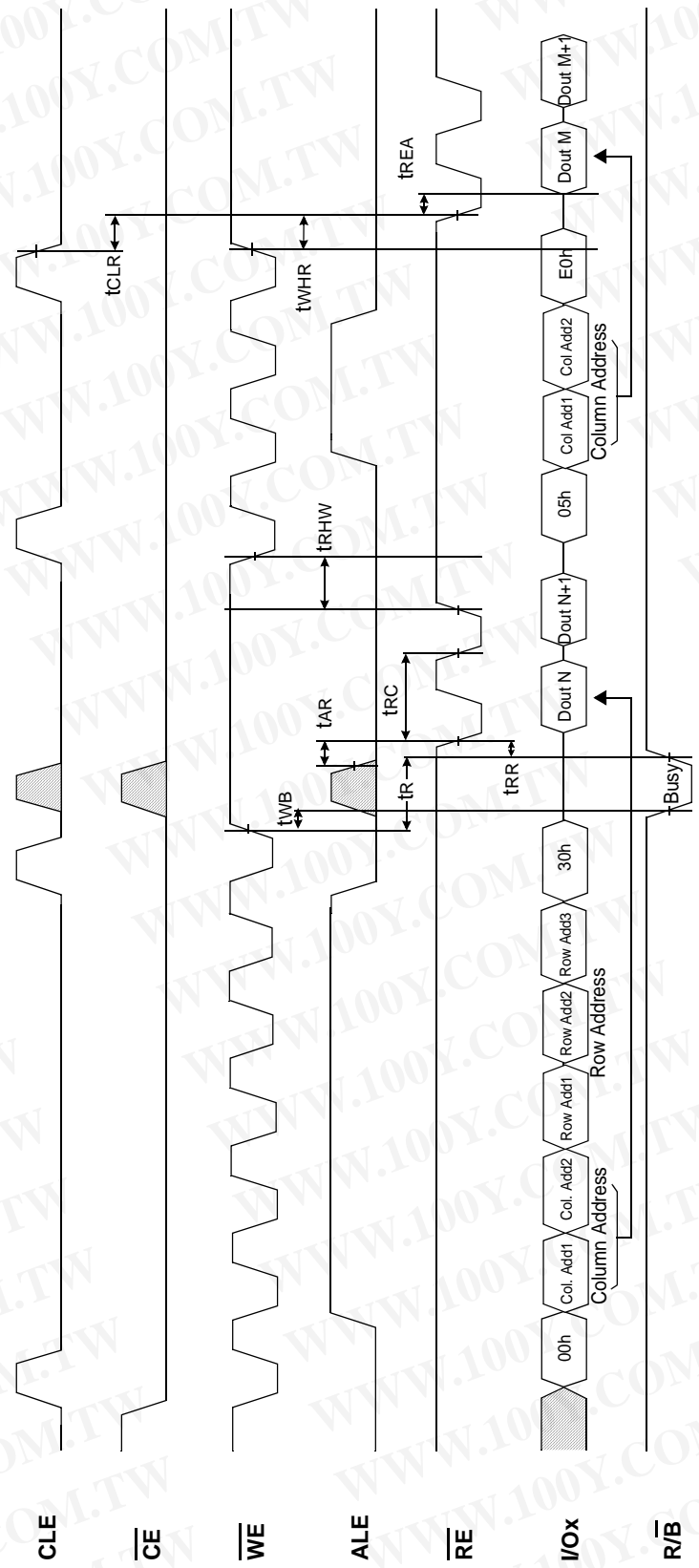


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**K9L8G08U1A**  
**K9G4G08U0A K9G4G08B0A**

**Preliminary**  
**FLASH MEMORY**

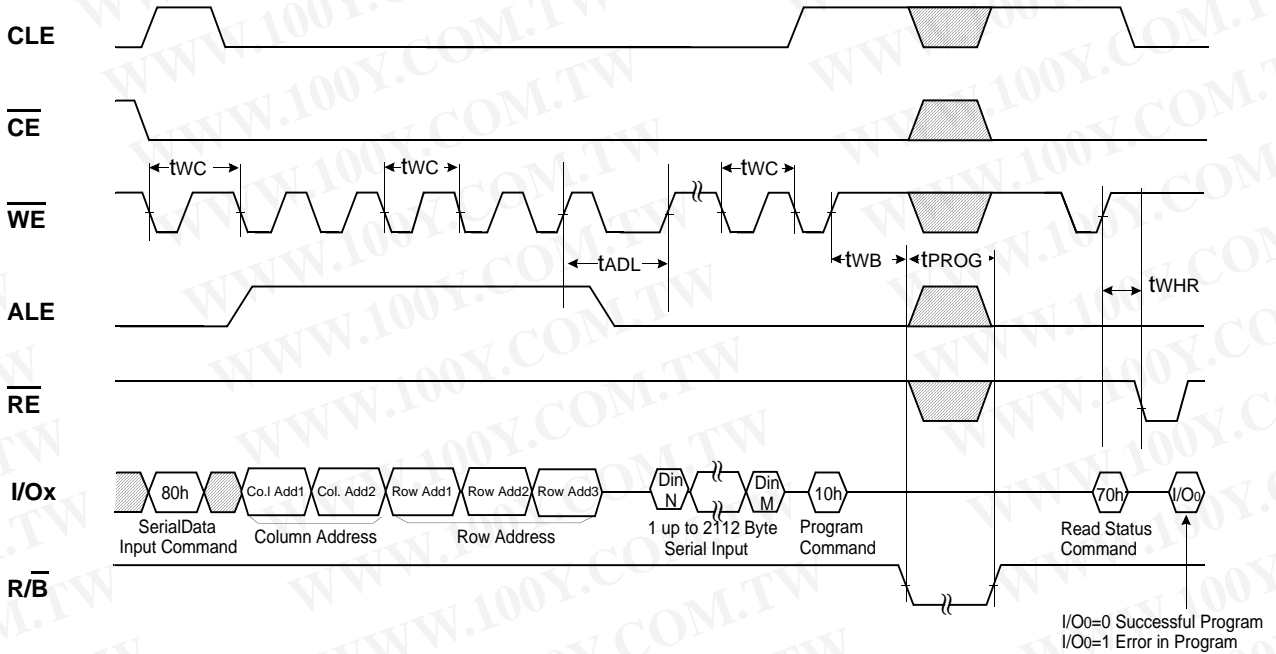
**Random Data Output In a Page**



**K9L8G08U1A  
K9G4G08U0A K9G4G08B0A**

**Preliminary  
FLASH MEMORY**

**Page Program Operation**



**NOTES :**  $t_{ADL}$  is the time from the  $\overline{WE}$  rising edge of final address cycle to the  $\overline{WE}$  rising edge of first data cycle.

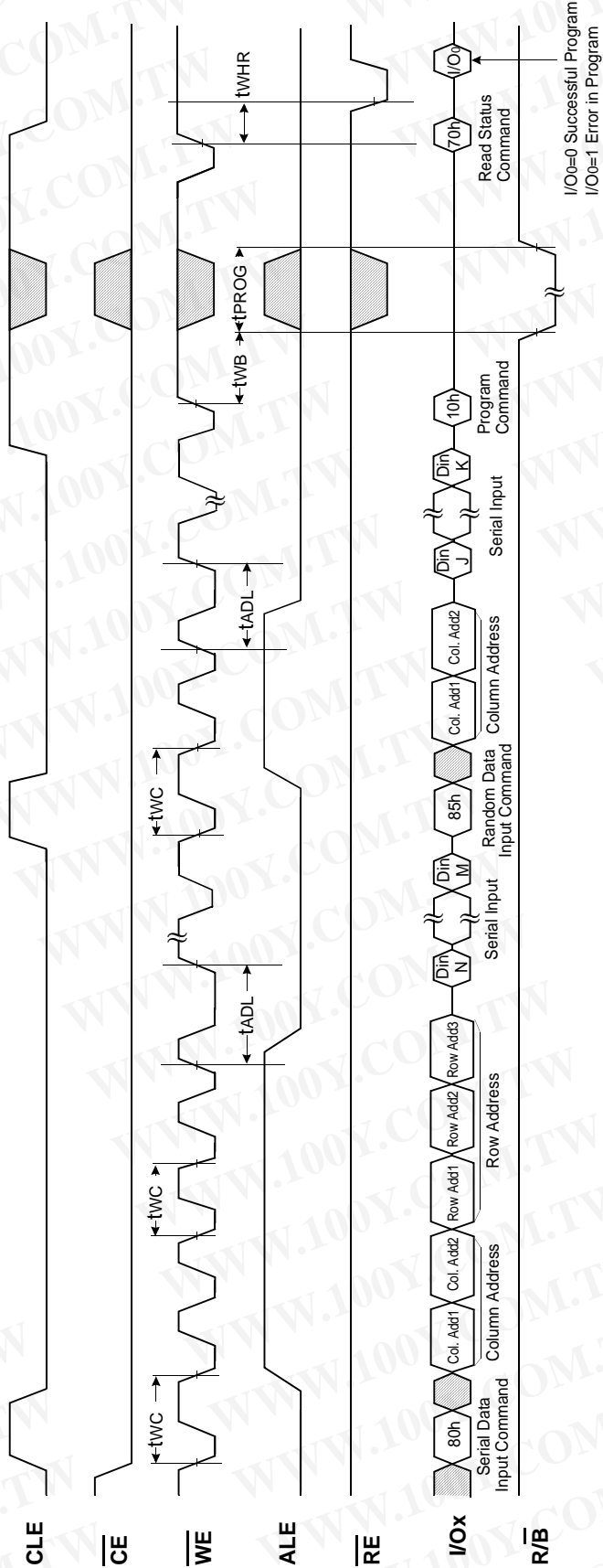
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K9L8G08U1A  
 K9G4G08U0A K9G4G08B0A

**Preliminary**  
**FLASH MEMORY**

Page Program Operation with Random Data Input



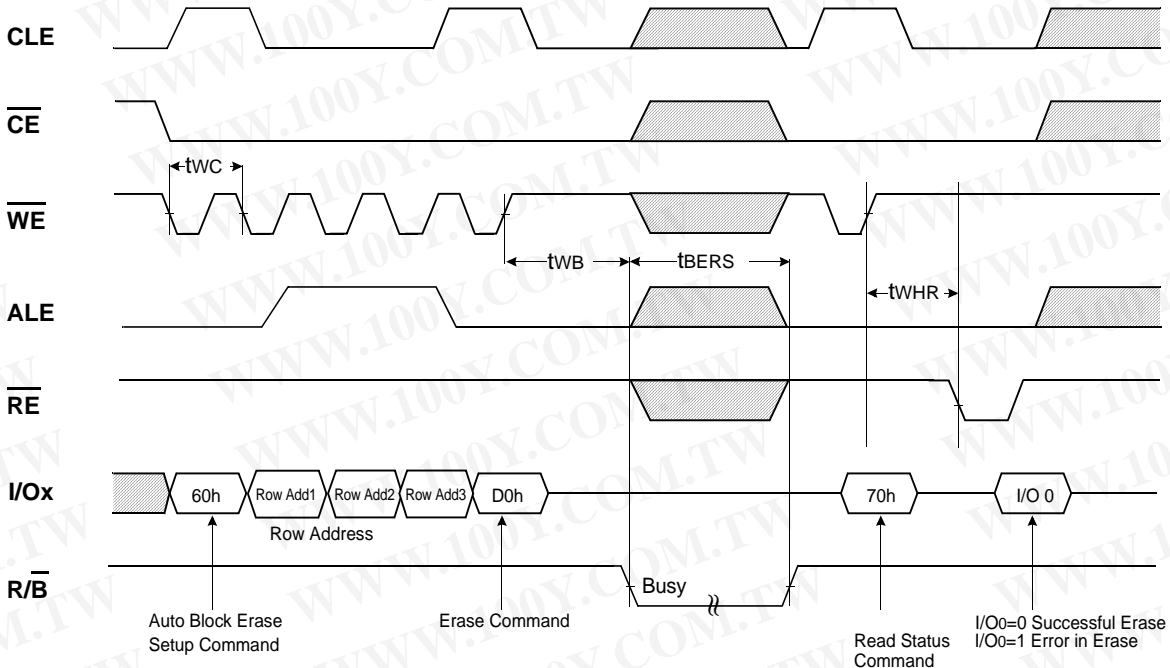
NOTES : tADL is the time from the WE rising edge of final address cycle to the WE rising edge of first data cycle.



**K9L8G08U1A  
K9G4G08U0A K9G4G08B0A**

**Preliminary  
FLASH MEMORY**

**Block Erase Operation**

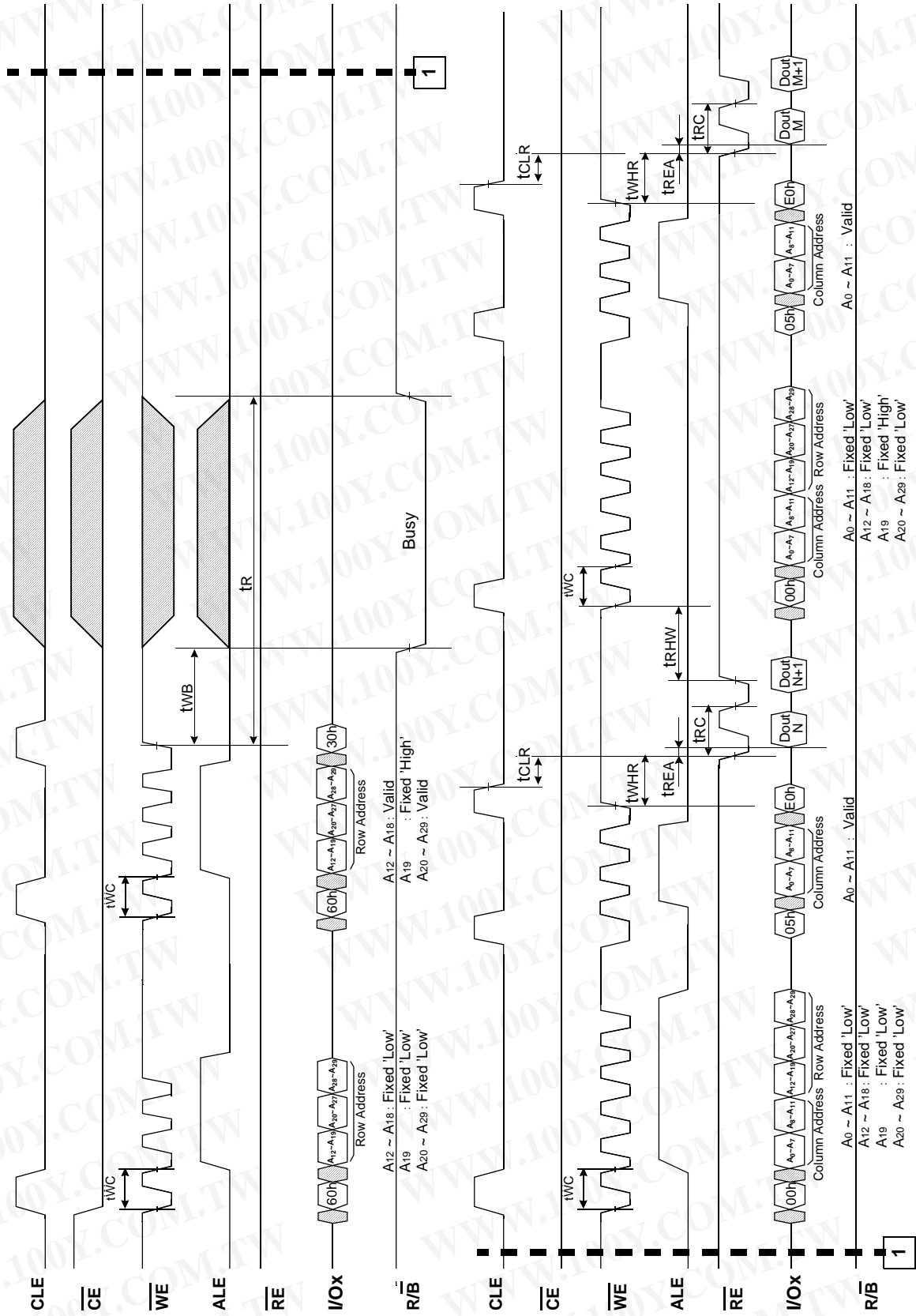


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**K9L8G08U1A**  
**K9G4G08U0A K9G4G08B0A**

**Preliminary**  
**FLASH MEMORY**

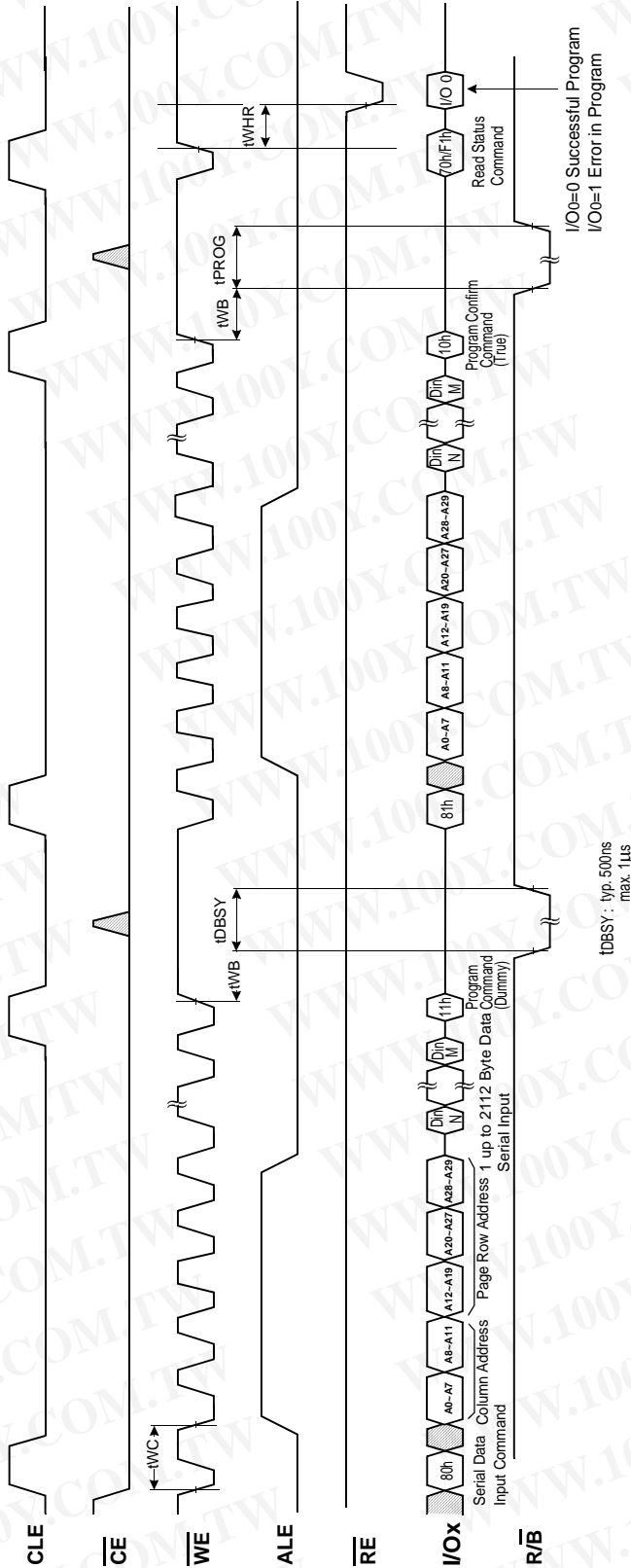
**Two-Plane Read Operation with Two-Plane Random Data Out**



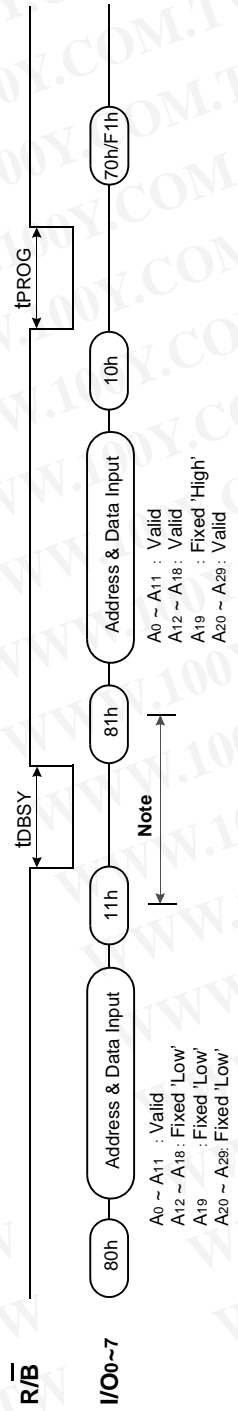
**K9L8G08U1A**  
**K9G4G08U0A K9G4G08B0A**

**Preliminary**  
**FLASH MEMORY**

**Two-Plane Page Program Operation**



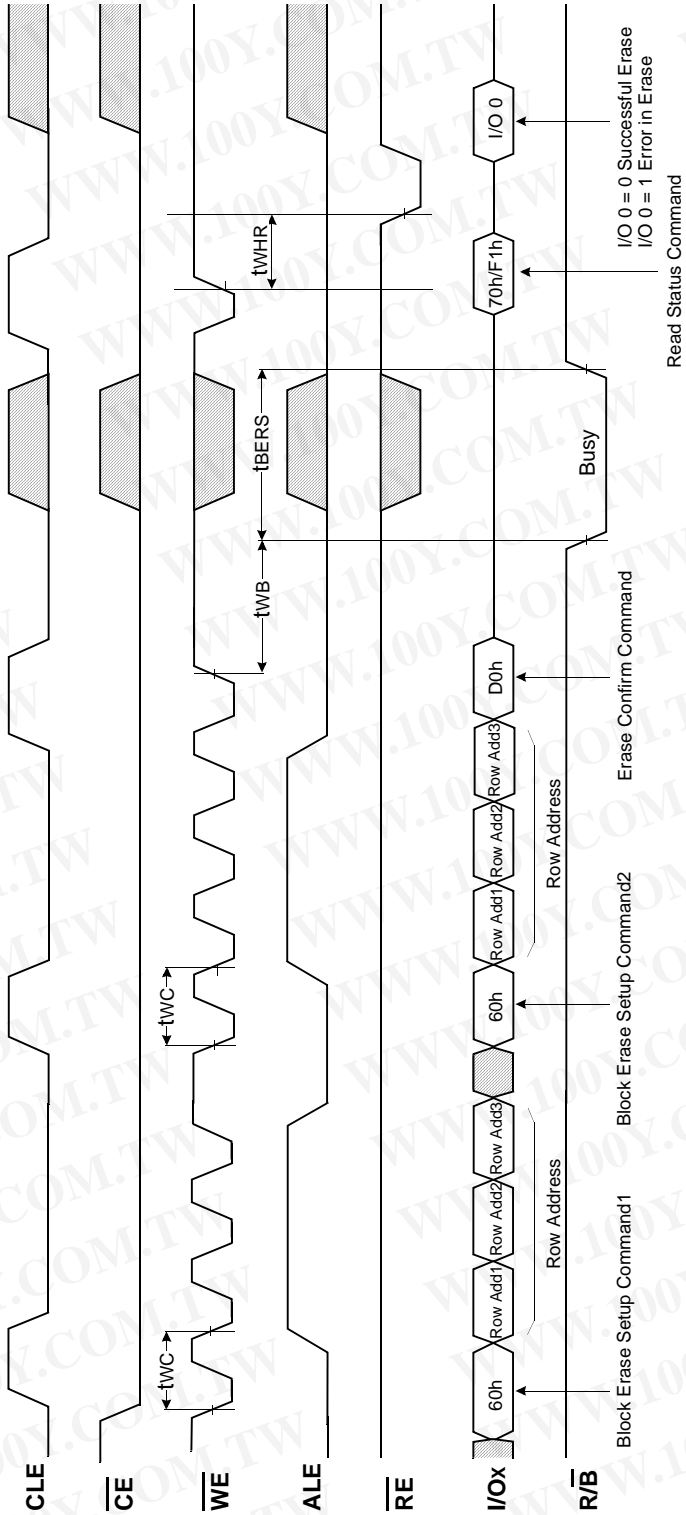
**Ex.) Two-Plane Page Program**



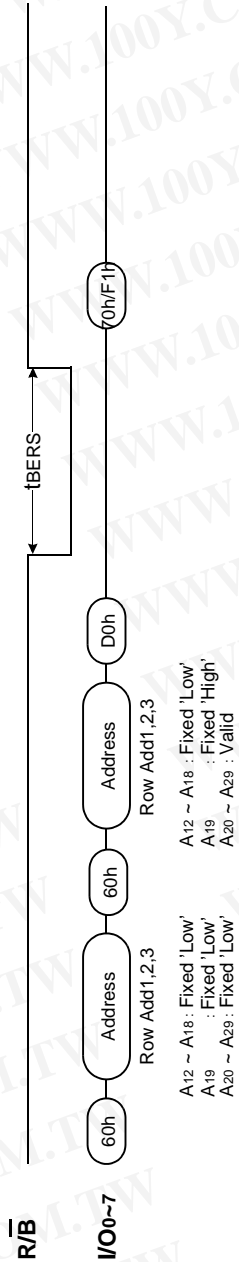
**Note:** Any command between 11h and 81h is prohibited except 70h/F1h and FFh.

**K9L8G08U1A  
 K9G4G08U0A K9G4G08B0A**

**Two-Plane Block Erase Operation**



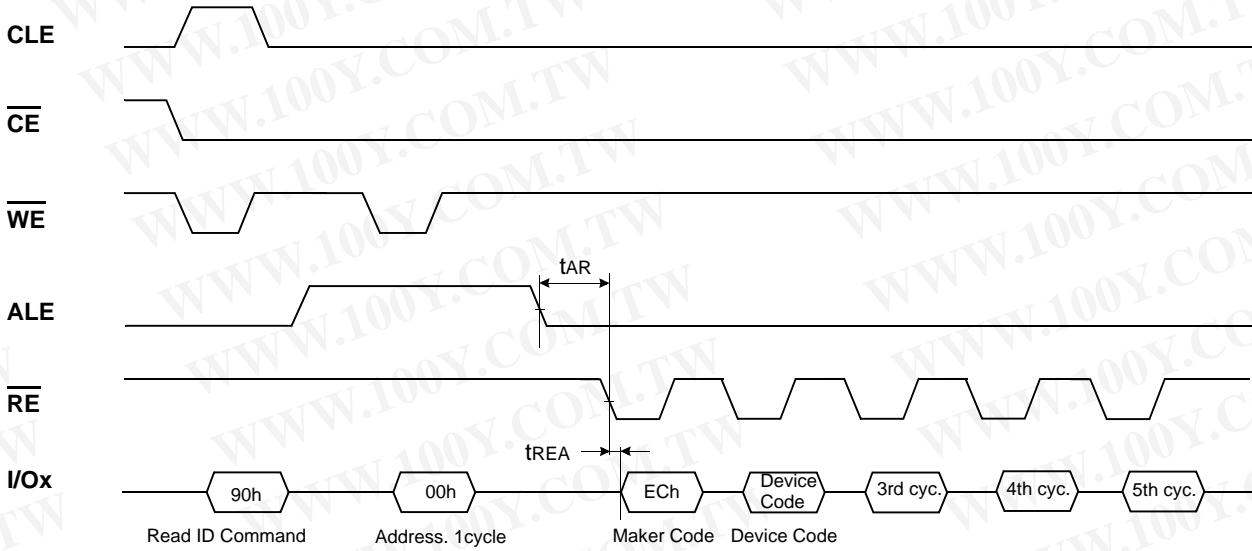
**Ex.) Address Restriction for Two-Plane Block Erase Operation**



**K9L8G08U1A  
K9G4G08U0A K9G4G08B0A**

**Preliminary  
FLASH MEMORY**

**Read ID Operation**



| Device     | Device Code(2nd Cycle)        | 3rd Cycle | 4th Cycle | 5th Cycle |
|------------|-------------------------------|-----------|-----------|-----------|
| K9G4G08B0A | DCh                           | 14h       | 25h       | 54h       |
| K9G4G08U0A | DCh                           | 14h       | 25h       | 54h       |
| K9L8G08U1A | Same as each K9G4G08U0A in it |           |           |           |

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**K9L8G08U1A**  
**K9G4G08U0A K9G4G08B0A**
**Preliminary**  
**FLASH MEMORY**
**ID Definition Table**
**90 ID : Access command = 90H**

|                      | Description   |
|----------------------|---|
| 1 <sup>st</sup> Byte | Maker Code  |
| 2 <sup>nd</sup> Byte | Device Code   |
| 3 <sup>rd</sup> Byte | Internal Chip Number, Cell Type, Number of Simultaneously Programed Pages, etc  |
| 4 <sup>th</sup> Byte | Page Size, Block Size, Redundant Area Size, Organization, Serial Access Minimum |
| 5 <sup>th</sup> Byte | Plane Number, Plane Size  |

**3rd ID Data**

|   | Description   | I/O7 | I/O6 | I/O5 | I/O4 | I/O3 | I/O2 | I/O1 | I/O0 |
|---|---------------|------|------|------|------|------|------|------|------|
| Internal Chip Number                      | 1             |      |      |      |      |      |      | 0    | 0    |
|   | 2             |      |      |      |      |      |      | 0    | 1    |
|   | 4             |      |      |      |      |      |      | 1    | 0    |
|   | 8             |      |      |      |      |      |      | 1    | 1    |
| Cell Type                                 | 2 Level Cell  |      |      |      |      | 0    | 0    |      |      |
|   | 4 Level Cell  |      |      |      |      | 0    | 1    |      |      |
|   | 8 Level Cell  |      |      |      |      | 1    | 0    |      |      |
|   | 16 Level Cell |      |      |      |      | 1    | 1    |      |      |
| Number of Simultaneously Programed Pages  | 1             |      |      | 0    | 0    |      |      |      |      |
|   | 2             |      |      | 0    | 1    |      |      |      |      |
|   | 4             |      |      | 1    | 0    |      |      |      |      |
|   | 8             |      |      | 1    | 1    |      |      |      |      |
| Interleave Program Between multiple chips | Not Support   |      | 0    |      |      |      |      |      |      |
|   | Support       |      | 1    |      |      |      |      |      |      |
| Cache Program                             | Not Support   | 0    |      |      |      |      |      |      |      |
|   | Support       | 1    |      |      |      |      |      |      |      |

**4th ID Data**

|                                     | Description | I/O7 | I/O6 | I/O5 | I/O4 | I/O3 | I/O2 | I/O1 | I/O0 |
|-------------------------------------|-------------|------|------|------|------|------|------|------|------|
| Page Size (w/o redundant area )     | 1KB         |      |      |      |      |      |      | 0    | 0    |
|                                     | 2KB         |      |      |      |      |      |      | 0    | 1    |
|                                     | 4KB         |      |      |      |      |      |      | 1    | 0    |
|                                     | 8KB         |      |      |      |      |      |      | 1    | 1    |
| Block Size (w/o redundant area )    | 64KB        |      |      | 0    | 0    |      |      |      |      |
|                                     | 128KB       |      |      | 0    | 1    |      |      |      |      |
|                                     | 256KB       |      |      | 1    | 0    |      |      |      |      |
|                                     | 512KB       |      |      | 1    | 1    |      |      |      |      |
| Redundant Area Size ( byte/512byte) | 8           |      |      |      |      |      | 0    |      |      |
|                                     | 16          |      |      |      |      |      | 1    |      |      |
| Organization                        | x8          |      | 0    |      |      |      |      |      |      |
|                                     | x16         |      | 1    |      |      |      |      |      |      |
| Serial Access Minimum               | 50ns/30ns   | 0    |      |      |      | 0    |      |      |      |
|                                     | 25ns        | 1    |      |      |      | 0    |      |      |      |
|                                     | Reserved    | 0    |      |      |      | 1    |      |      |      |
|                                     | Reserved    | 1    |      |      |      | 1    |      |      |      |

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**K9L8G08U1A**  
**K9G4G08U0A K9G4G08B0A**
**Preliminary**  
**FLASH MEMORY**
**5th ID Data**

|                                    | Description | I/O7 | I/O6 | I/O5 | I/O4 | I/O3 | I/O2 | I/O1 | I/O0 |
|------------------------------------|-------------|------|------|------|------|------|------|------|------|
| Plane Number                       | 1           |      |      |      |      | 0    | 0    |      |      |
|                                    | 2           |      |      |      |      | 0    | 1    |      |      |
|                                    | 4           |      |      |      |      | 1    | 0    |      |      |
|                                    | 8           |      |      |      |      | 1    | 1    |      |      |
| Plane Size<br>(w/o redundant Area) | 64Mb        |      | 0    | 0    | 0    |      |      |      |      |
|                                    | 128Mb       |      | 0    | 0    | 1    |      |      |      |      |
|                                    | 256Mb       |      | 0    | 1    | 0    |      |      |      |      |
|                                    | 512Mb       |      | 0    | 1    | 1    |      |      |      |      |
|                                    | 1Gb         |      | 1    | 0    | 0    |      |      |      |      |
|                                    | 2Gb         |      | 1    | 0    | 1    |      |      |      |      |
|                                    | 4Gb         |      | 1    | 1    | 0    |      |      |      |      |
| 8Gb                                |             | 1    | 1    | 1    |      |      |      |      |      |
| Reserved                           |             | 0    |      |      |      |      |      | 0    | 0    |

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**Preliminary  
FLASH MEMORY**

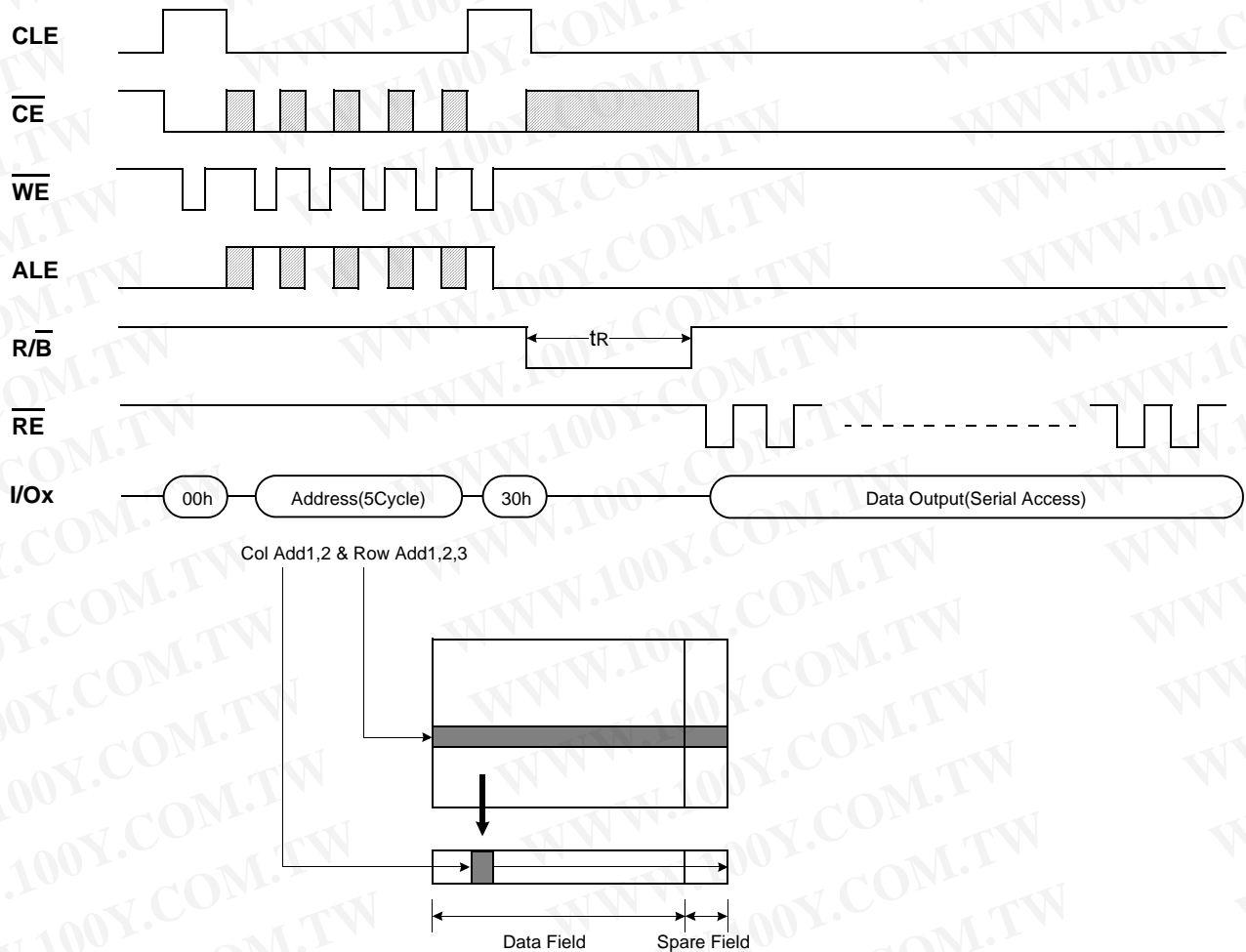
**Device Operation**

**PAGE READ**

Page read is initiated by writing 00h-30h to the command register along with five address cycles. After initial power up, 00h command is latched. Therefore only five address cycles and 30h command initiates that operation after initial power up. The 2,112 bytes of data within the selected page are transferred to the data registers in less than 60μs( $t_R$ ). The system controller can detect the completion of this data transfer( $t_R$ ) by analyzing the output of R/B pin. Once the data in a page is loaded into the data registers, they may be read out in 30ns cycle time by sequentially pulsing RE. The repetitive high to low transitions of the RE clock make the device output the data starting from the selected column address up to the last column address.

The device may output random data in a page instead of the consecutive sequential data by writing random data output command. The column address of next data, which is going to be out, may be changed to the address which follows random data output command. Random data output can be operated multiple times regardless of how many times it is done in a page.

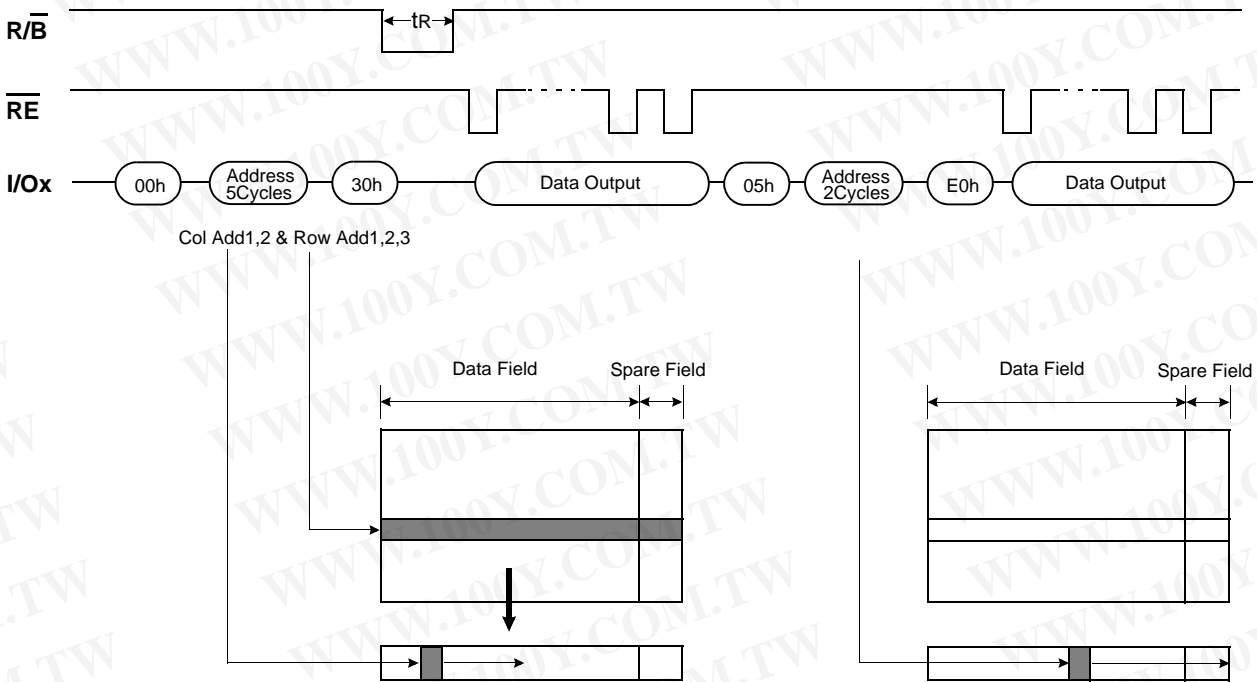
**Figure 6. Read Operation**



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**K9L8G08U1A  
 K9G4G08U0A K9G4G08B0A**

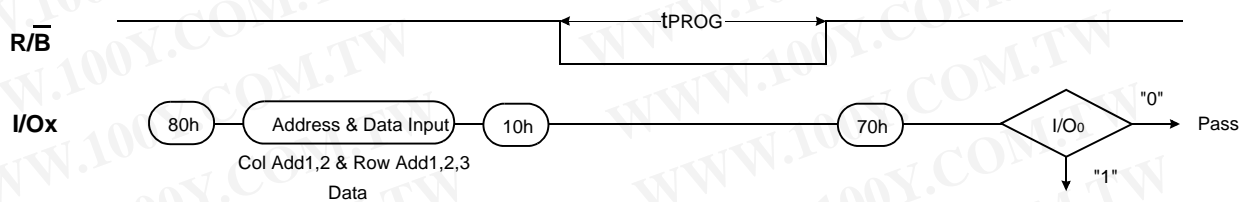
**Figure 7. Random Data Output In a Page**



**PAGE PROGRAM**

The device is programmed basically on a page basis, and the number of consecutive partial page programming operation within the same page without an intervening erase operation must not exceed 1 time for the page. The addressing should be done in sequential order in a block. A page program cycle consists of a serial data loading period in which up to 2,112bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. The serial data loading period begins by inputting the Serial Data Input command(80h), followed by the five cycle address inputs and then serial data loading. The data other than those to be programmed do not need to be loaded. The device supports random data input in a page. The column address for the next data, which will be entered, may be changed to the address which follows random data input command(85h). Random data input may be operated multiple times regardless of how many times it is done in a page. The Page Program confirm command(10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal write state controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/B output, or the Status bit(I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit(I/O 0) may be checked(Figure 8). The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

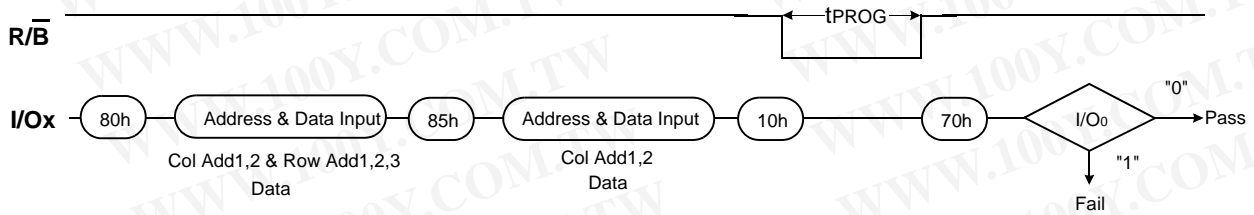
**Figure 8. Program & Read Status Operation**



**K9L8G08U1A**  
**K9G4G08U0A K9G4G08B0A**

**Preliminary**  
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**Figure 9. Random Data Input In a Page**



**Table 2. Paired Page Address Information**

| Paired Page Address |     | Paired Page Address |     |
|---------------------|-----|---------------------|-----|
| 00h                 | 04h | 01h                 | 05h |
| 02h                 | 08h | 03h                 | 09h |
| 06h                 | 0Ch | 07h                 | 0Dh |
| 0Ah                 | 10h | 0Bh                 | 11h |
| 0Eh                 | 14h | 0Fh                 | 15h |
| 12h                 | 18h | 13h                 | 19h |
| 16h                 | 1Ch | 17h                 | 1Dh |
| 1Ah                 | 20h | 1Bh                 | 21h |
| 1Eh                 | 24h | 1Fh                 | 25h |
| 22h                 | 28h | 23h                 | 29h |
| 26h                 | 2Ch | 27h                 | 2Dh |
| 2Ah                 | 30h | 2Bh                 | 31h |
| 2Eh                 | 34h | 2Fh                 | 35h |
| 32h                 | 38h | 33h                 | 39h |
| 36h                 | 3Ch | 37h                 | 3Dh |
| 3Ah                 | 40h | 3Bh                 | 41h |
| 3Eh                 | 44h | 3Fh                 | 45h |
| 42h                 | 48h | 43h                 | 49h |
| 46h                 | 4Ch | 47h                 | 4Dh |
| 4Ah                 | 50h | 4Bh                 | 51h |
| 4Eh                 | 54h | 4Fh                 | 55h |
| 52h                 | 58h | 53h                 | 59h |
| 56h                 | 5Ch | 57h                 | 5Dh |
| 5Ah                 | 60h | 5Bh                 | 61h |
| 5Eh                 | 64h | 5Fh                 | 65h |
| 62h                 | 68h | 63h                 | 69h |
| 66h                 | 6Ch | 67h                 | 6Dh |
| 6Ah                 | 70h | 6Bh                 | 71h |
| 6Eh                 | 74h | 6Fh                 | 75h |
| 72h                 | 78h | 73h                 | 79h |
| 76h                 | 7Ch | 77h                 | 7Dh |
| 7Ah                 | 7Eh | 7Bh                 | 7Fh |

**Note:** When program operation is abnormally aborted (ex. power-down), not only page data under program but also paired page data may be damaged(Table 2).

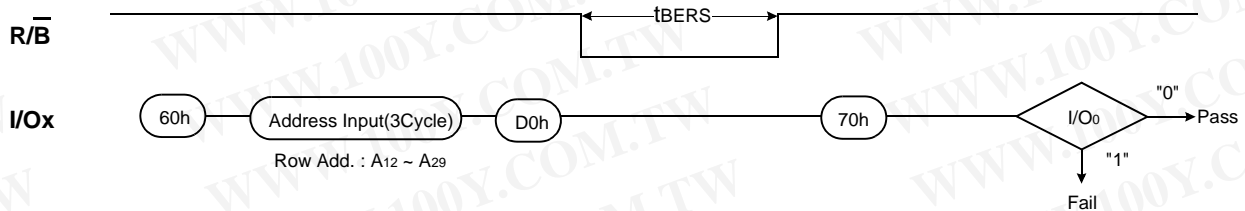
**K9L8G08U1A**  
**K9G4G08U0A K9G4G08B0A**

**BLOCK ERASE**

The Erase operation is done on a block basis. Block address loading is accomplished in three cycles initiated by an Erase Setup command(60h). Only address A19 to A29 is valid while A12 to A18 is ignored. The Erase Confirm command(D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.

At the rising edge of  $\overline{WE}$  after the erase confirm command input, the internal write controller handles erase and erase-verify. When the erase operation is completed, the Write Status Bit(I/O 0) may be checked. Figure 10 details the sequence.

**Figure 10. Block Erase Operation**



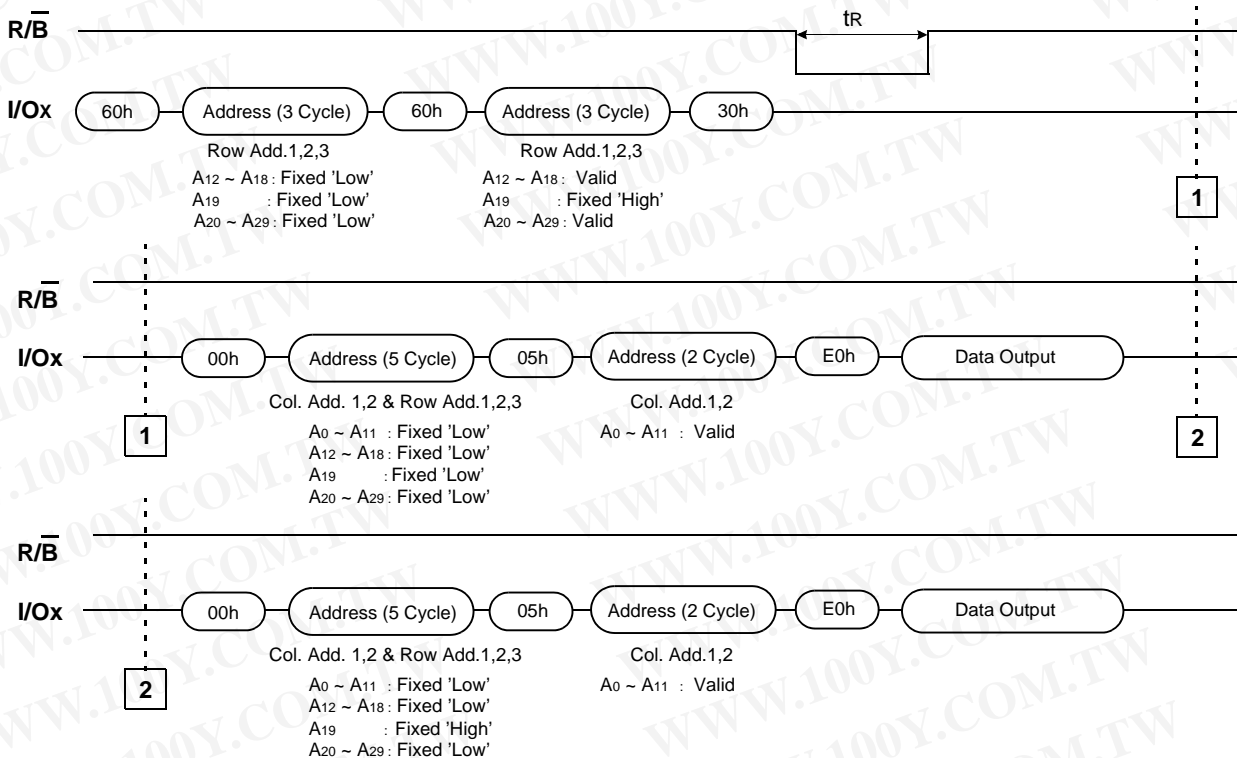
**Two-Plane Read**

Two-Plane Read is an extension of Read, for a single plane with 2,112 byte page registers. Since the device is equipped with two memory planes, activating the two sets of 2,112 byte page registers enables a random read of two pages. Two-Plane Read is initiated by repeating command 60h followed by three address cycles twice. In this case only same page of same block can be selected from each plane.

After Read Confirm command(30h) the 4,224 bytes of data within the selected two page are transferred to the data registers in less than 60us(tR). The system controller can detect the completion of data transfer(tR) by monitoring the output of  $\overline{R/B}$  pin.

Once the data is loaded into the data registers, the data output of first plane can be read out by issuing command 00h with Five Address Cycles, command 05h with two column address and finally E0h. The data output of second plane can be read out using the identical command sequences. The restrictions in addressing with Two-Plane Read are shown in Figure 11. Two-Plane Read must be used in the block which has been programmed with Two-Plane Page Program.

**Figure 11. Two-Plane Page Read Operation with Two-Plane Random Data Out**



**K9L8G08U1A  
K9G4G08U0A K9G4G08B0A**

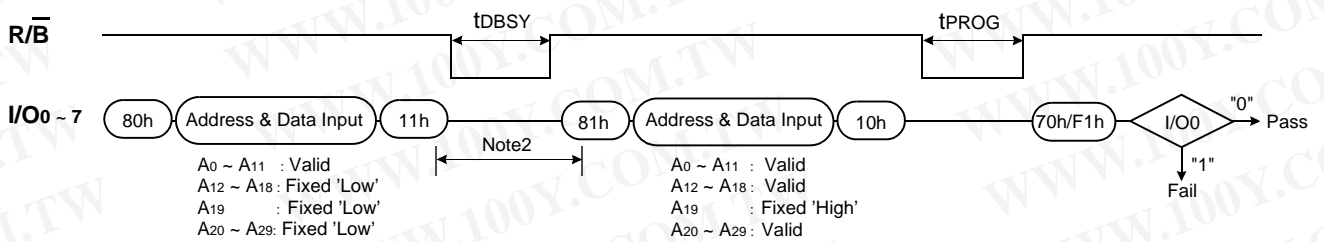
**Preliminary  
FLASH MEMORY**

**Two-Plane Page Program**

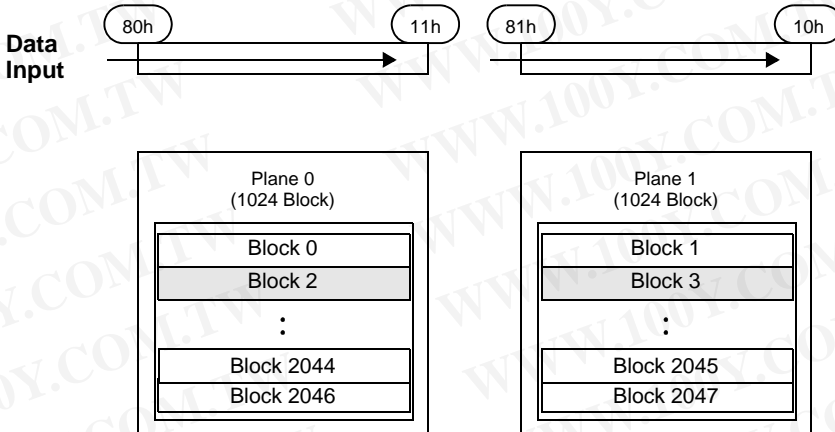
Two-Plane Page Program is an extension of Page Program, for a single plane with 2112 byte page registers. Since the device is equipped with two memory planes, activating the two sets of 2112 byte page registers enables a simultaneous programming of two pages.

After writing the first set of data up to 2112 byte into the selected page register, Dummy Page Program command (11h) instead of actual Page Program command(10h) is inputted to finish data-loading of the first plane. Since no programming process is involved, R/B remains in Busy state for a short period of time(tDBSY). Read Status command (70h) may be issued to find out when the device returns to Ready state by polling the Ready/Busy status bit(I/O 6). Then the next set of data for the other plane is inputted after the 81h command and address sequences. After inputting data for the last plane, actual True Page Program command(10h) instead of dummy Page Program command (11h) must be followed to start the programming process. The operation of R/B and Read Status is the same as that of Page Program. Status bit of I/O 0 is set to "1" when any of the pages fails. Restriction in addressing with Two-Plane Page Program is shown in Figure12.

**Figure 12. Two-Plane Page Program**



**NOTE :** 1. It is noticeable that physically same row address is applied to two planes.  
2. Any command between 11h and 81h is prohibited except 70h/F1h and FFh.



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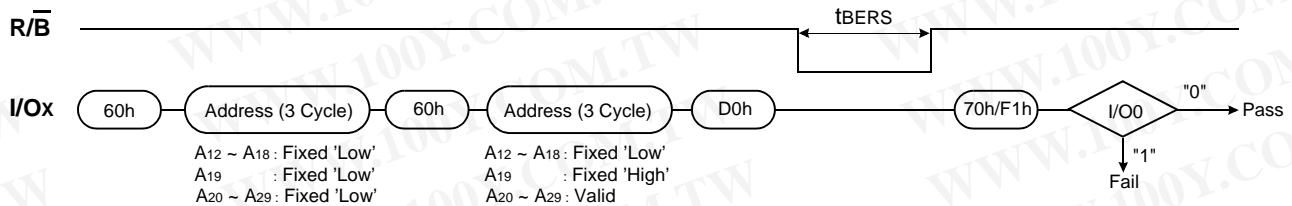
## K9L8G08U1A K9G4G08U0A K9G4G08B0A

## Preliminary FLASH MEMORY

### Two-Plane Block Erase

Basic concept of Two-Plane Block Erase operation is identical to that of Two-Plane Page Program. Up to two blocks, one from each plane can be simultaneously erased. Standard Block Erase command sequences (Block Erase Setup command(60h) followed by three address cycles) may be repeated up to twice for erasing up to two blocks. Only one block should be selected from each plane. The Erase Confirm command(D0h) initiates the actual erasing process. The completion is detected by monitoring R/ $\bar{B}$  pin or Ready/Busy status bit (I/O 6).

Figure 13. Two-Plane Erase Operation



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**K9L8G08U1A**  
**K9G4G08U0A K9G4G08B0A**
**Preliminary**  
**FLASH MEMORY**
**READ STATUS**

The device contains a Status Register which may be read to find out whether program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h or F1h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of  $\overline{CE}$  or  $\overline{RE}$ , whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/B pins are common-wired.  $\overline{RE}$  or  $\overline{CE}$  does not need to be toggled for updated status. Refer to Table 3 for specific 70h Status Register definitions and Table 4 for specific F1h Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, the read command(00h) should be given before starting read cycles.

**Table 3. 70h Read Status Register Definition**

| I/O No. | Page Program  | Block Erase   | Read          | Definition                               |
|---------|---------------|---------------|---------------|--|
| I/O 0   | Pass/Fail     | Pass/Fail     | Not use       | Pass : "0"      Fail : "1"               |
| I/O 1   | Not use       | Not use       | Not use       | Don't -cared                             |
| I/O 2   | Not use       | Not use       | Not use       | Don't -cared                             |
| I/O 3   | Not Use       | Not Use       | Not Use       | Don't -cared                             |
| I/O 4   | Not Use       | Not Use       | Not Use       | Don't -cared                             |
| I/O 5   | Not Use       | Not Use       | Not Use       | Don't -cared                             |
| I/O 6   | Ready/Busy    | Ready/Busy    | Ready/Busy    | Busy : "0"      Ready : "1"              |
| I/O 7   | Write Protect | Write Protect | Write Protect | Protected : "0"      Not Protected : "1" |

**NOTE :** 1. I/Os defined 'Not use' are recommended to be masked out when Read Status is being executed.

**Table 4. F1h Read Status Register Definition**

| I/O No. | Page Program     | Block Erase      | Read          | Definition                               |
|---------|------------------|------------------|---------------|--|
| I/O 0   | Chip Pass/Fail   | Chip Pass/Fail   | Not use       | Pass : "0"      Fail : "1"               |
| I/O 1   | Plane0 Pass/Fail | Plane0 Pass/Fail | Not use       | Pass : "0"      Fail : "1"               |
| I/O 2   | Plane1 Pass/Fail | Plane1 Pass/Fail | Not use       | Pass : "0"      Fail : "1"               |
| I/O 3   | Not Use          | Not Use          | Not Use       | Don't -cared                             |
| I/O 4   | Not Use          | Not Use          | Not Use       | Don't -cared                             |
| I/O 5   | Not Use          | Not Use          | Not Use       | Don't -cared                             |
| I/O 6   | Ready/Busy       | Ready/Busy       | Ready/Busy    | Busy : "0"      Ready : "1"              |
| I/O 7   | Write Protect    | Write Protect    | Write Protect | Protected : "0"      Not Protected : "1" |

**NOTE :** 1. I/Os defined 'Not use' are recommended to be masked out when Read Status is being executed.

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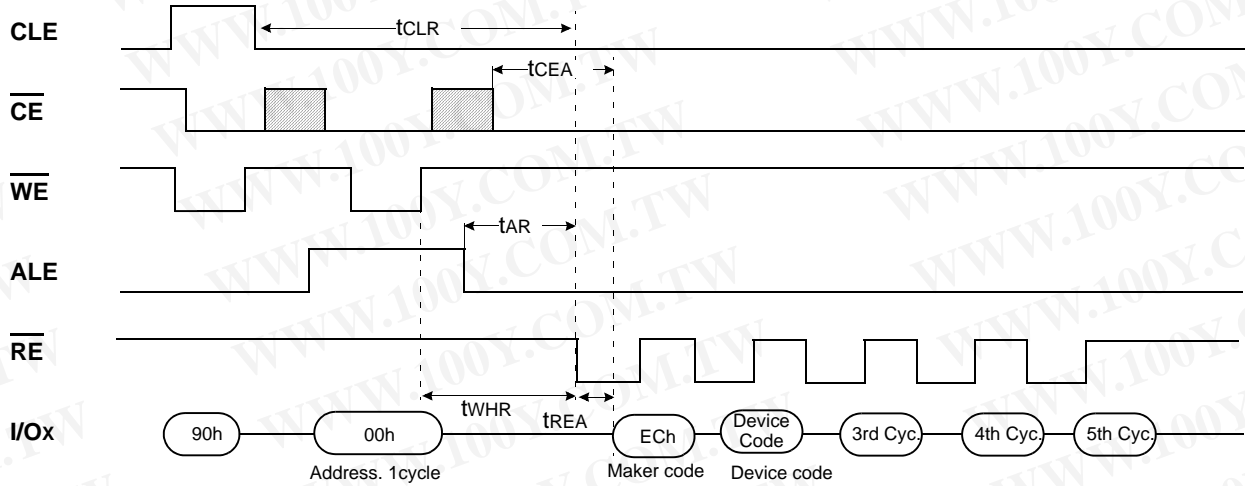
**K9L8G08U1A  
K9G4G08U0A K9G4G08B0A**

**Preliminary  
FLASH MEMORY**

**Read ID**

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Five read cycles sequentially output the manufacturer code(ECh), and the device code and 3rd cycle ID, 4th cycle ID, 5th cycle ID respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 14 shows the operation sequence.

**Figure 14. Read ID Operation**

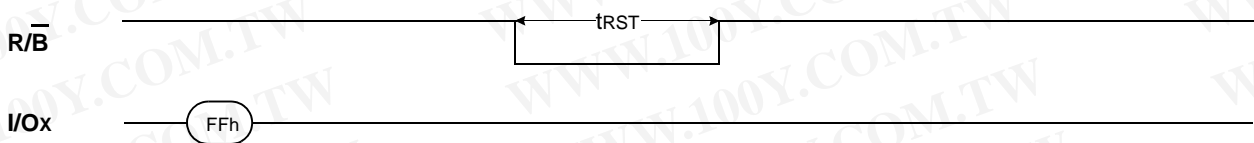


| Device     | Device Code(2nd Cycle)        | 3rd Cycle | 4th Cycle | 5th Cycle |
|------------|-------------------------------|-----------|-----------|-----------|
| K9G4G08B0A | DCh                           | 14h       | 25h       | 54h       |
| K9G4G08U0A | DCh                           | 14h       | 25h       | 54h       |
| K9L8G08U1A | Same as each K9G4G08X0A in it |           |           |           |

**RESET**

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when WP is high. Refer to Table 5 for device status after reset operation. If the device is already in reset state a new reset command will be accepted by the command register. The R/B pin changes to low for tRST after the Reset command is written. Refer to Figure 15 below.

**Figure 15. RESET Operation**



**Table 5. Device Status**

|                | After Power-up         | After Reset              |
|----------------|------------------------|--------------------------|
| Operation mode | 00h Command is latched | Waiting for next command |

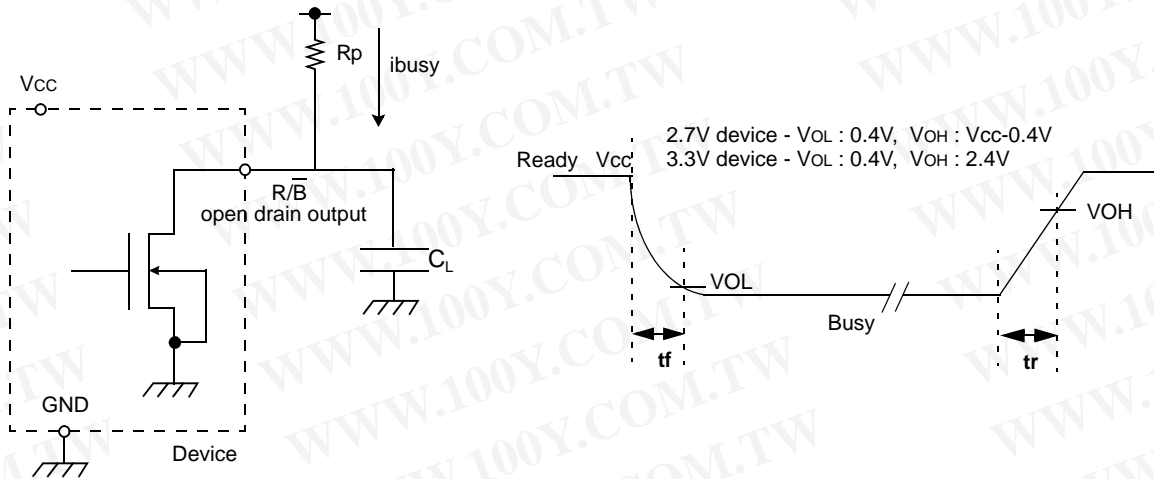
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# K9L8G08U1A K9G4G08U0A K9G4G08B0A

## Preliminary FLASH MEMORY

### READY/BUSY

The device has a  $\overline{R/B}$  output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The  $\overline{R/B}$  pin is normally high but transitions to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more  $\overline{R/B}$  outputs to be Or-tied. Because pull-up resistor value is related to  $t_r(\overline{R/B})$  and current drain during busy( $i_{busy}$ ), an appropriate value can be obtained with the following reference chart(Fig 16). Its value can be determined by the following guidance.

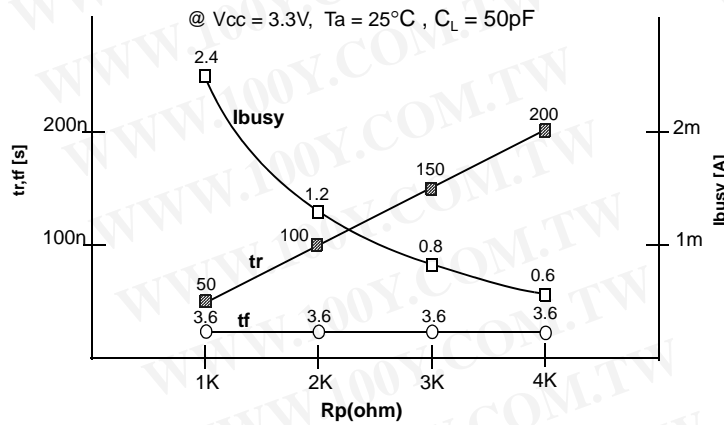
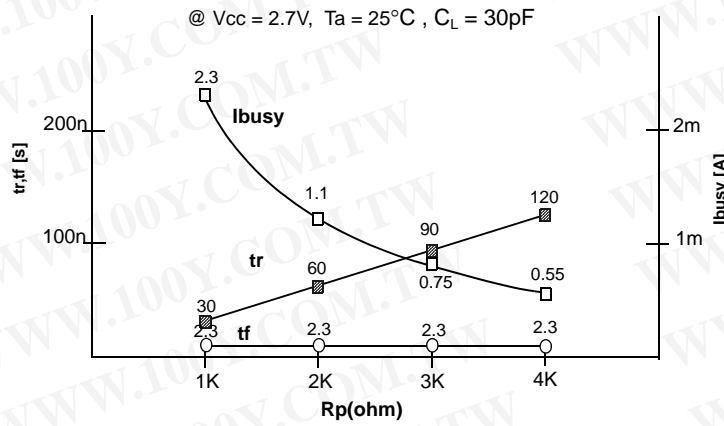


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**Preliminary  
FLASH MEMORY**

**Figure 16. Rp vs tr ,tf & Rp vs ibusy**



**Rp value guidance**

$$R_{p(\min, 2.7V \text{ part})} = \frac{V_{cc(\text{Max.})} - V_{OL(\text{Max.})}}{I_{OL} + \sum I_L} = \frac{2.4V}{3mA + \sum I_L}$$

$$R_{p(\min, 3.3V \text{ part})} = \frac{V_{cc(\text{Max.})} - V_{OL(\text{Max.})}}{I_{OL} + \sum I_L} = \frac{3.2V}{8mA + \sum I_L}$$

where IL is the sum of the input currents of all devices tied to the R/B pin.

Rp(max) is determined by maximum permissible limit of tr

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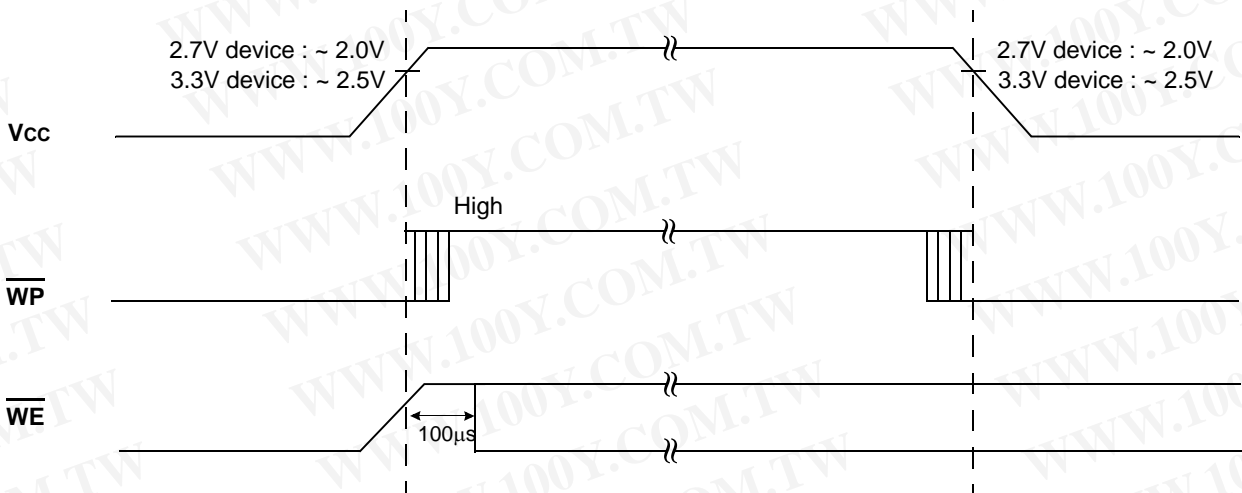
## K9L8G08U1A K9G4G08U0A K9G4G08B0A

## Preliminary FLASH MEMORY

### Data Protection & Power up sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever  $V_{CC}$  is below about 1.8V(2.7V device), 2V(3.3V device).  $\overline{WP}$  pin provides hardware protection and is recommended to be kept at  $V_{IL}$  during power-up and power-down. A recovery time of minimum 100 $\mu$ s is required before internal circuit gets ready for any command sequences as shown in Figure 17. The two step command sequence for program/erase provides additional software protection.

Figure 17. AC Waveforms for Power Transition



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**K9L8G08U1A  
K9G4G08U0A K9G4G08B0A**

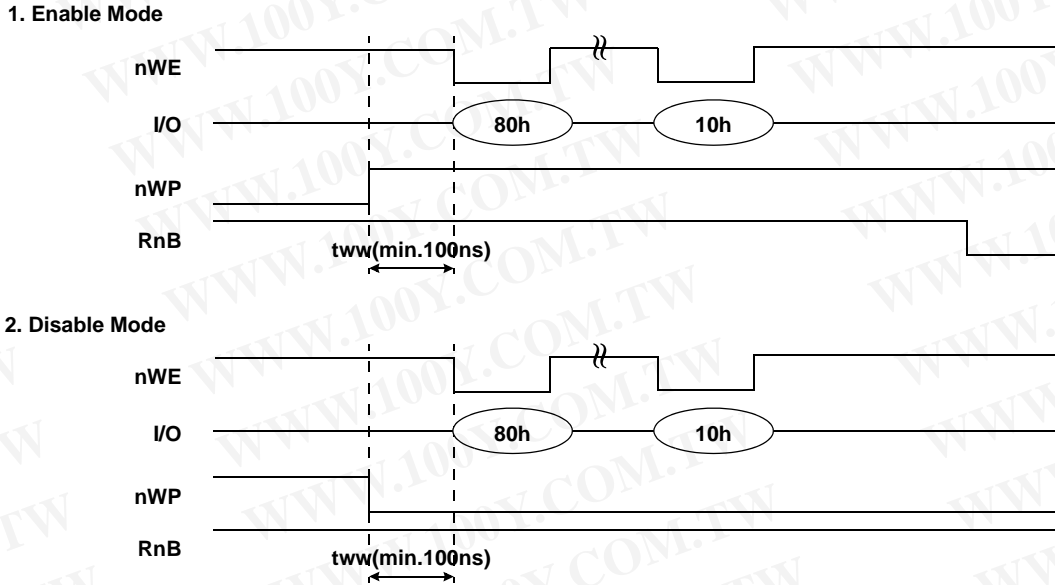
**Preliminary  
FLASH MEMORY**

**nWP AC Timing guide**

Enabling nWP during erase and program busy is prohibited.  
The erase and program operations are enabled and disabled as follows:

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**Figure 18. Program Operation**



**Figure 19. Erase Operation**

